Semiconductor Devices II

Part 2

Chapter 5: Beyond CMOS devices

Andras Kis

andras.kis@epfl.ch

EPFL – École Polytechnique Fédérale de Lausanne

Electrical Engineering Institute

[Outline] Chapter 5: Beyond CMOS devices

Fundamental limits to power dissipation

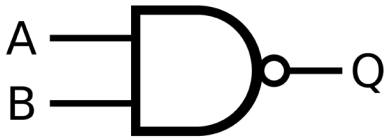
- Landauer limit
- Von Neumann architecture
- Joule heating

Emerging concepts based on 2D materials

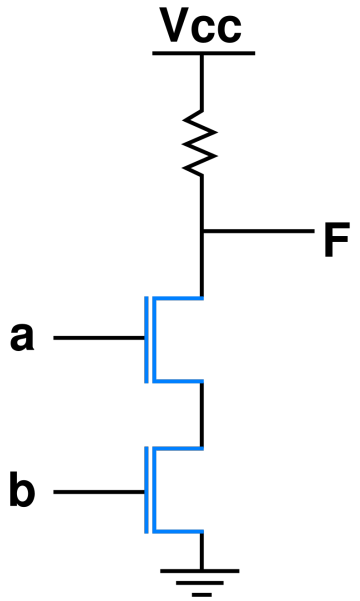
- Memory in logic
- Valley/spintronics
- Excitonic devices

Information processing, energy and reversibility

Consider the NAND logic gate and its truth table



A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



NMOS
NAND gate

Logically irreversible operation: 3 different input configurations give the same output ("1")

If we "destroy" the inputs and only keep the result, we have increased the entropy

Limits on computing: The Landauer limit

Erasure of N bits of information from a physical system results in:

- An increase in entropy of

  $$\Delta S \geq k_B \ln(2) \cdot N$$

- Energy dissipation of

  $$\Delta E \geq k_B T \ln(2) \cdot N$$

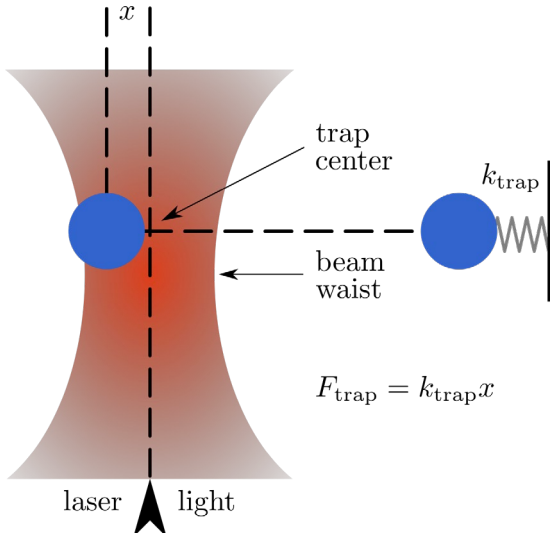
- For 1 bit:

  $$\Delta E \geq k_B T \ln(2) = 2.86 \cdot 10^{-21} J$$

Rolf Landauer, IBM J. Res. & Dev. (1961)

k_B Boltzmann constant
T temperature

Experimental verification of the Landauer principle



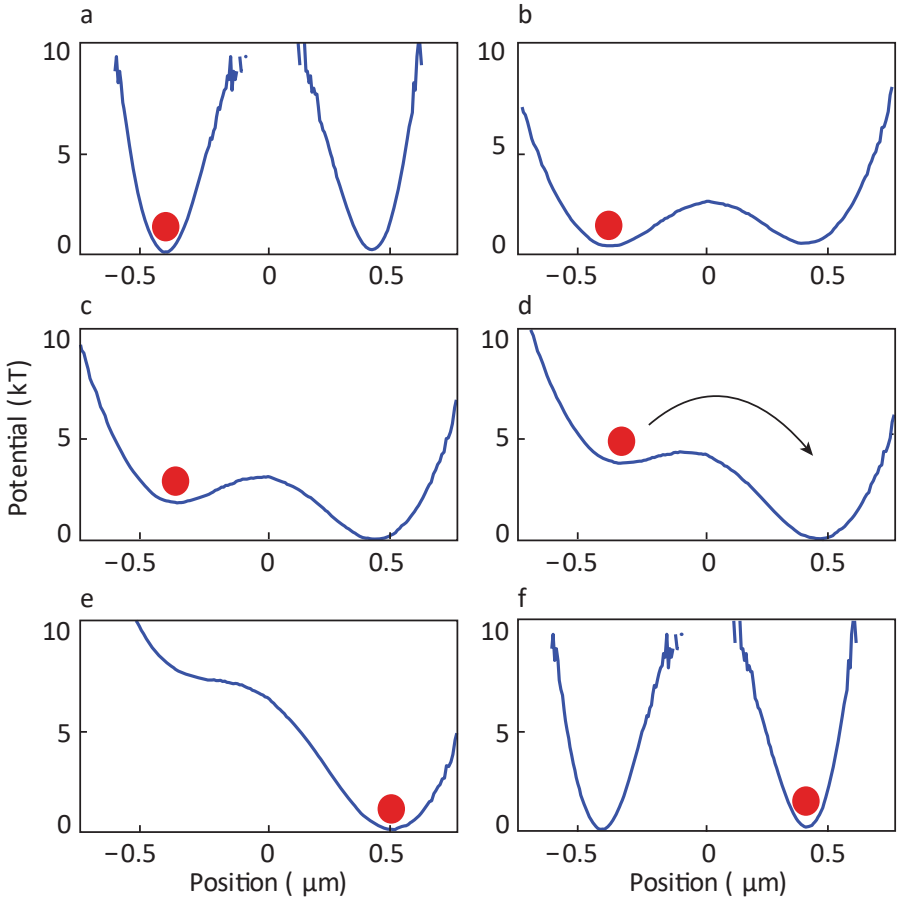
Source: Wikipedia

Particle in an optical tweezer, laser quickly moving between two positions, generating two nearby traps

Two states:

- Particle in left trap: 0
- Particle in right trap: 1

Erasure procedure

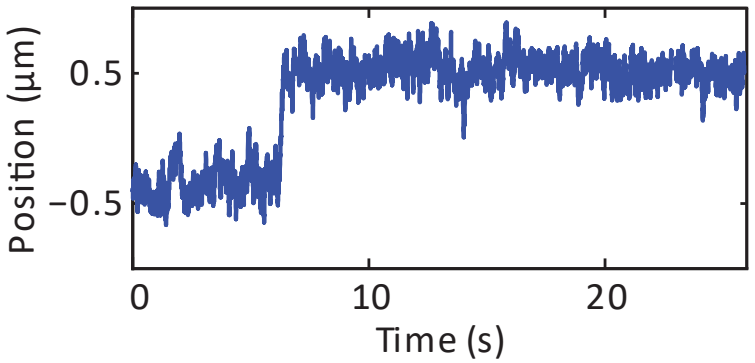


Bérut et al, Nature (2012)

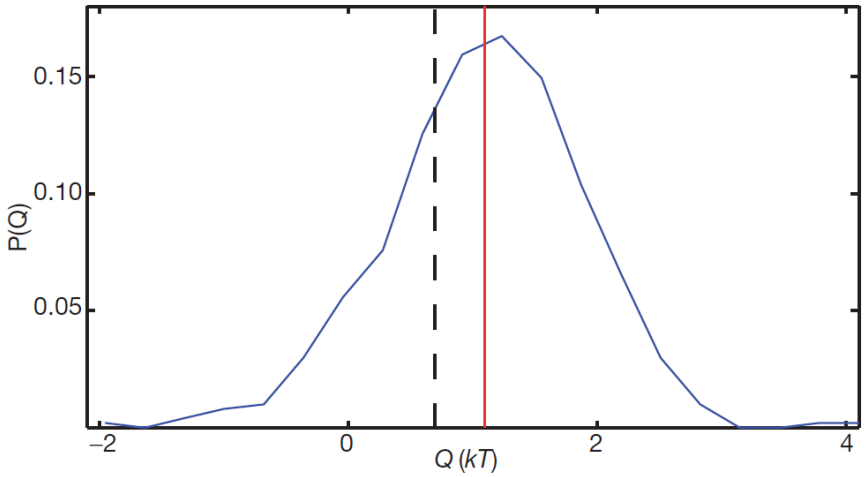
Information is erased: the state is reset to 1 (or 0) irrespective of the starting state

Experimental verification of the Landauer principle

Bead trajectory for 0 → 1 transition



Dissipated energy distribution

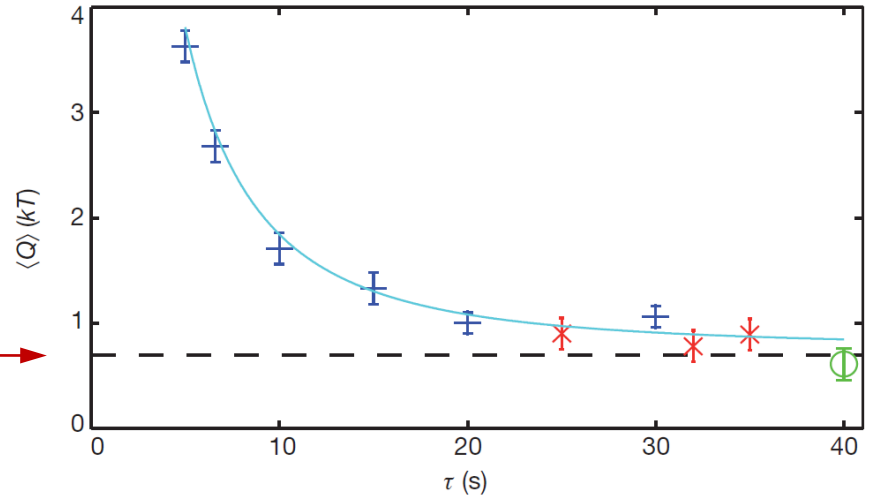


Dissipated energy:

$$Q = -\int_0^{\tau_{cycle}} dt F \cdot v =$$

$$= -\int_0^{\tau_{cycle}} dt \dot{x}\, \partial U/\partial x$$

Landauer limit →

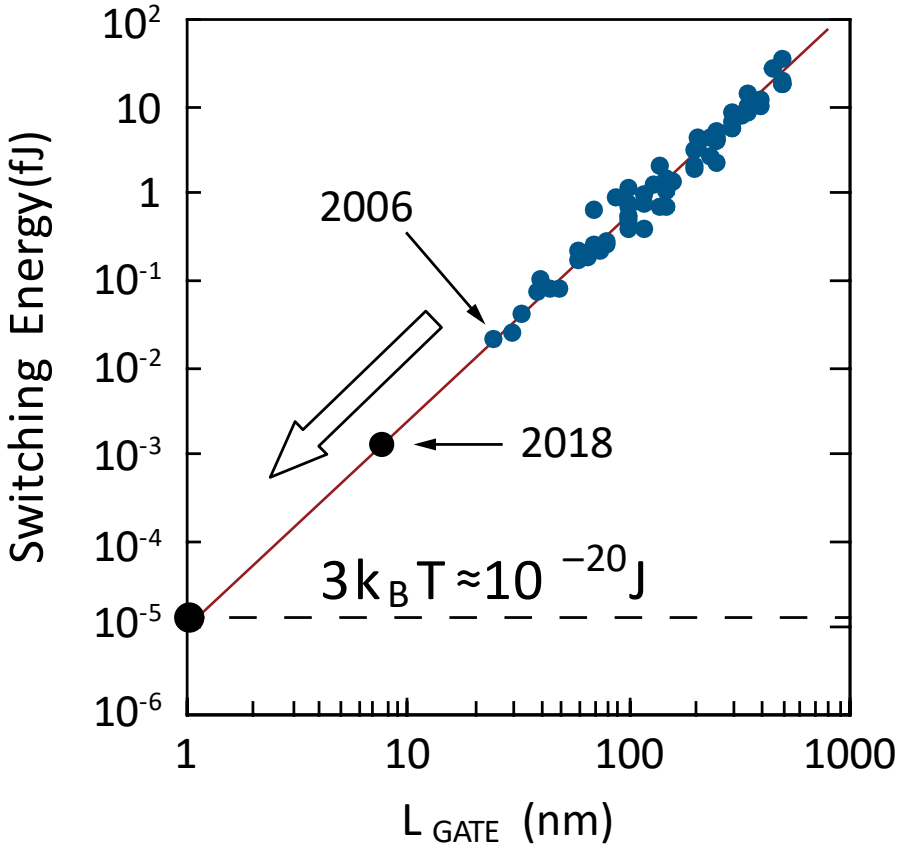


Bérut et al, Nature (2012)

Limits on switching

For a charge-based switch

- Minimum switching energy is: $\Delta E_{sw_{min}} = 3k_B \mathrm{T} \cdot \ln(2) \approx 10^{-20}\, J$
- ≈ 4× worse than Landauer



Cavin et al. J Nanopart Res (2006)

k_B Boltzmann constant
T temperature

How about the entire system?

Intel Core i7 8700K processor (2017)

- Benchmark: 217 GOPS
- Dissipated power: 86.2 W

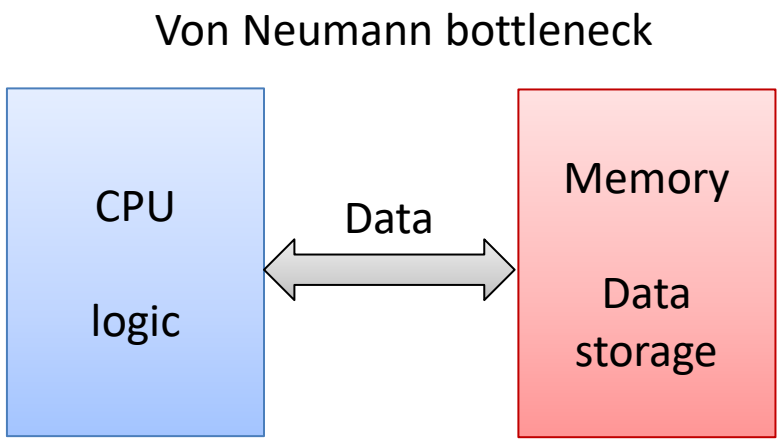
$$\frac{Dissipated\ power}{N\ operations} = \frac{86.2}{217 \cdot 10^9} = 3.97 \cdot 10^{-10}\,\frac{J}{flops}$$
$$= 6.2 \cdot 10^{-12}\,\frac{J}{ops}\ (64\ \text{bits})$$

- Landauer limit:

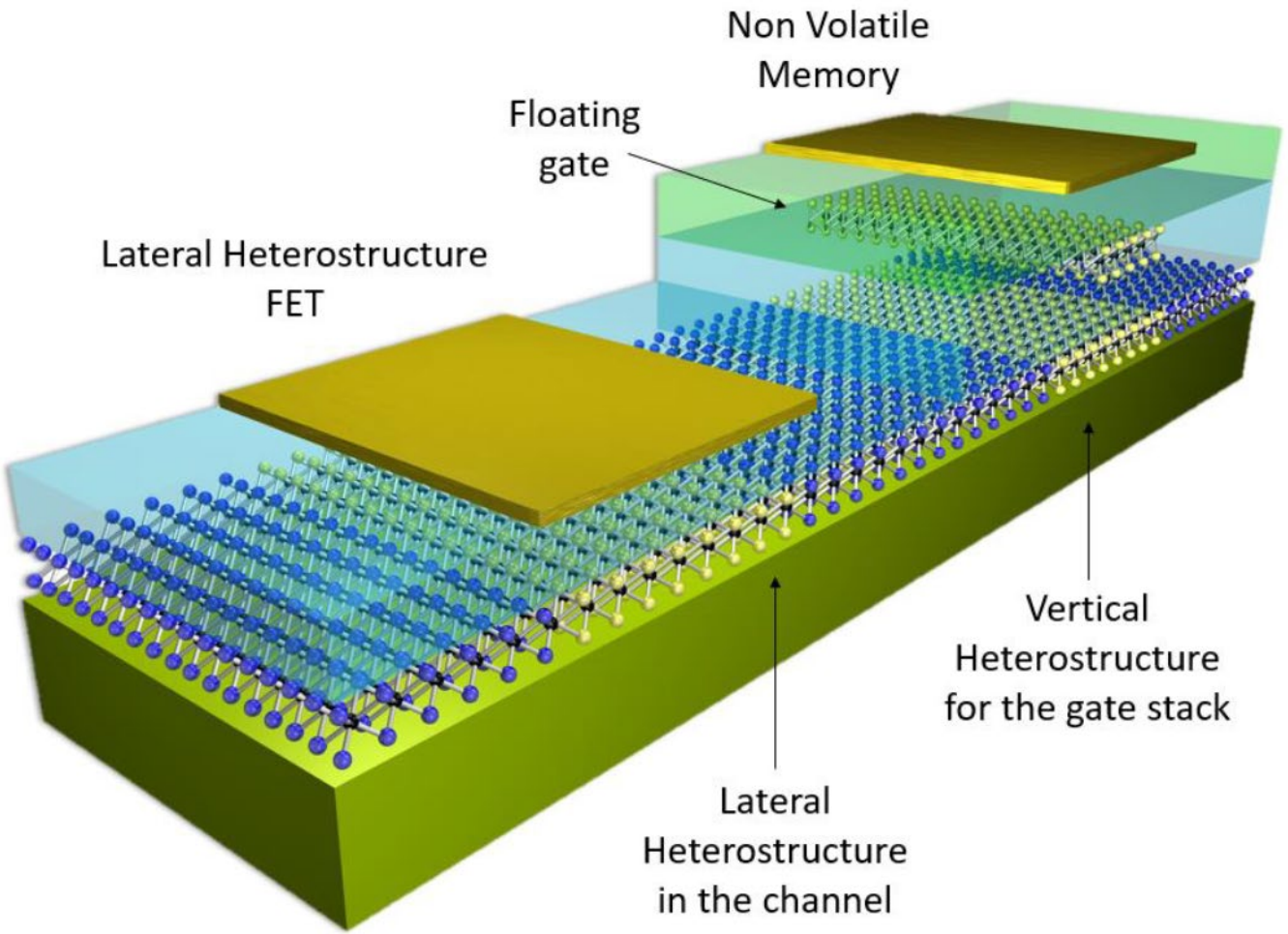
$$2.86 \cdot 10^{-21}\ J/ops$$

We are $10^9\times$ worse than the Landauer limit!

Von Neumann architecture



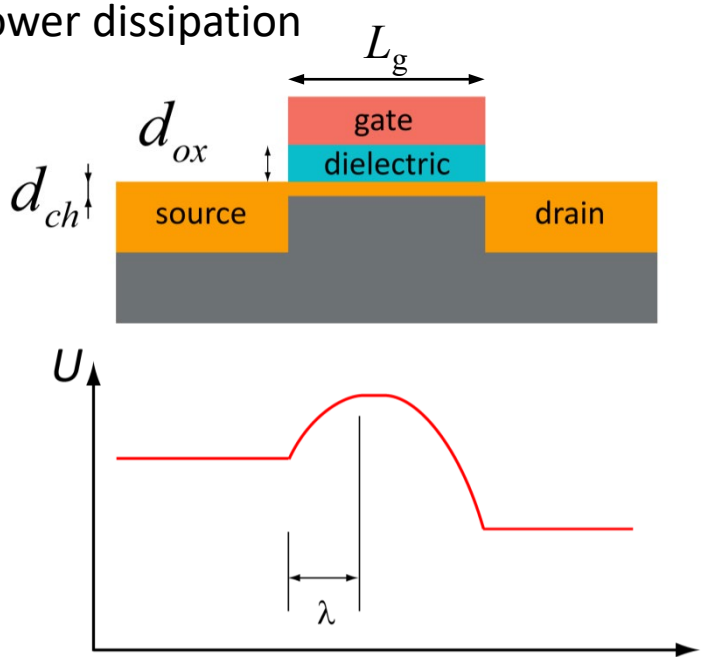
Logic in Memory Concept

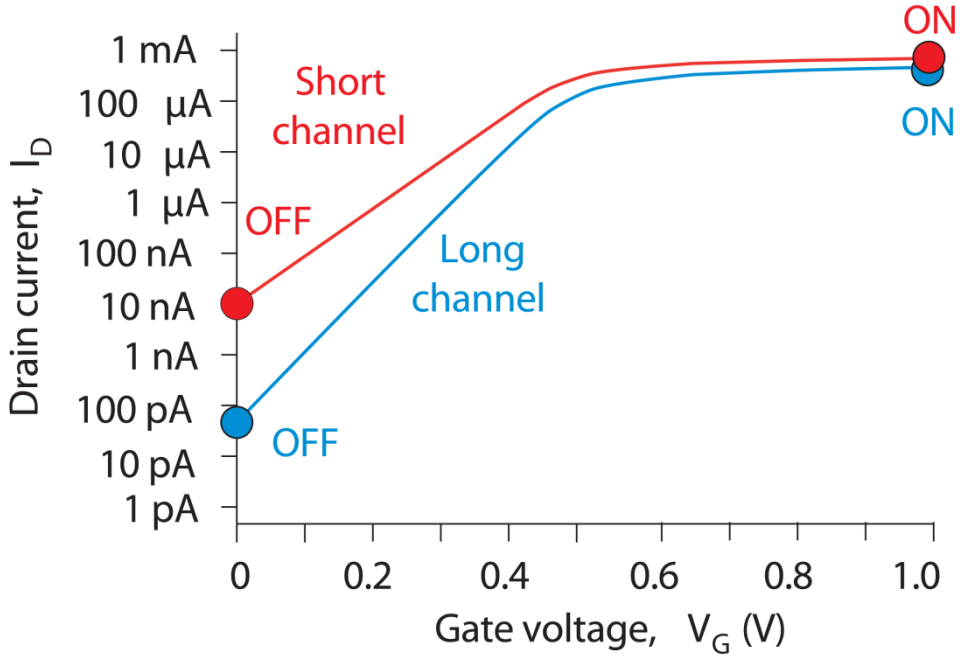


Credit: Giuseppe Iannaccone, University of Pisa

Ch 2.1: Heat Dissipation in Small Transistors

Planar MOSFET – short channel effects; standby power dissipation





$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} d_{ox} d_{ch}}$$

ε(Si)=11.9

To deplete the channel: L_g at least 3–5× λ

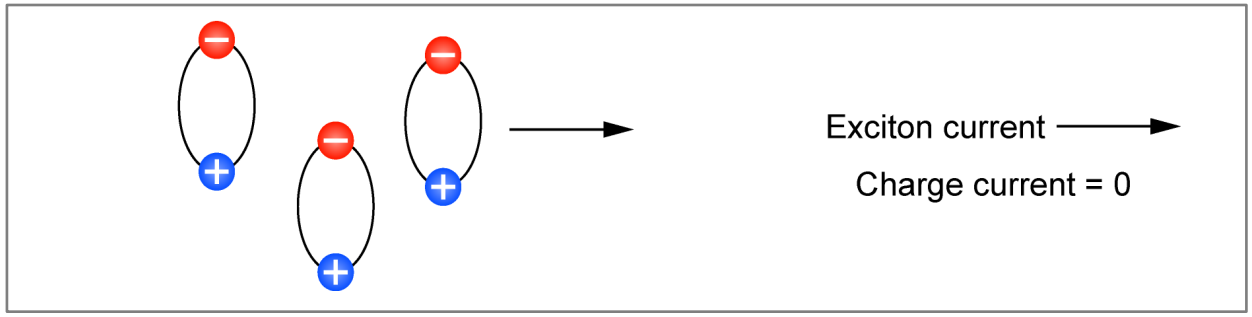
Example:

2nm thin Si, 1nm SiO_2: L_g>10nm

Ferain et al., Nature 479, 310 (2011)

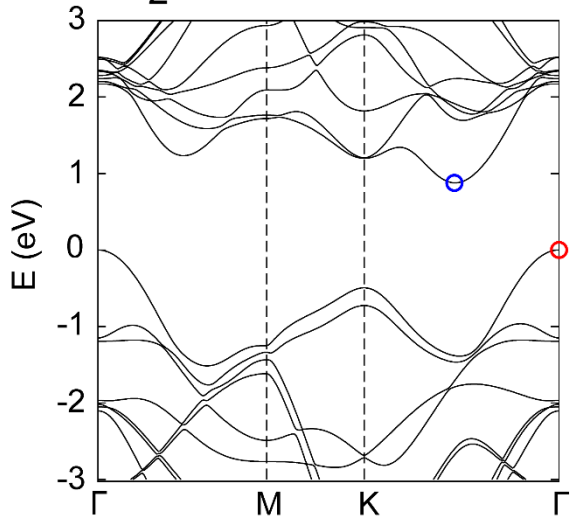
Colinge, Sol. State El. 48, 897 (2004)

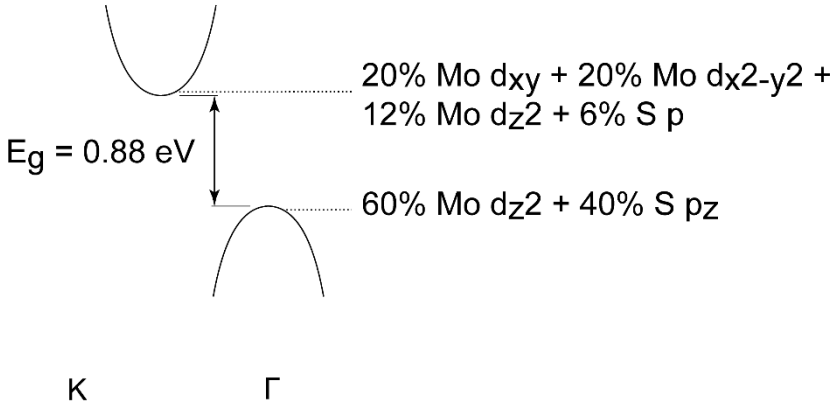
Other Types of Current



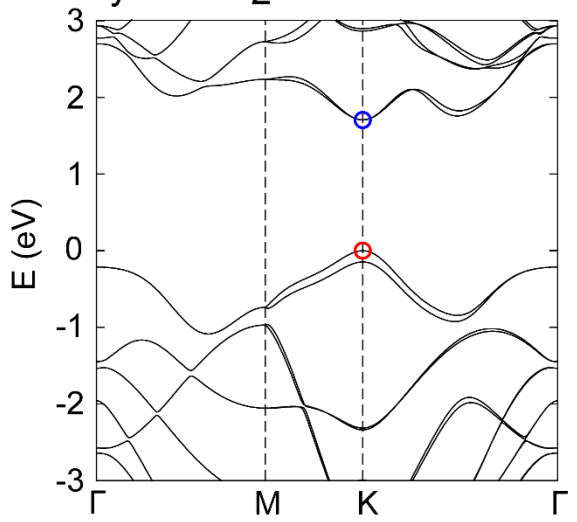
Ch 2.4: Band Structure of 2H MoS_2

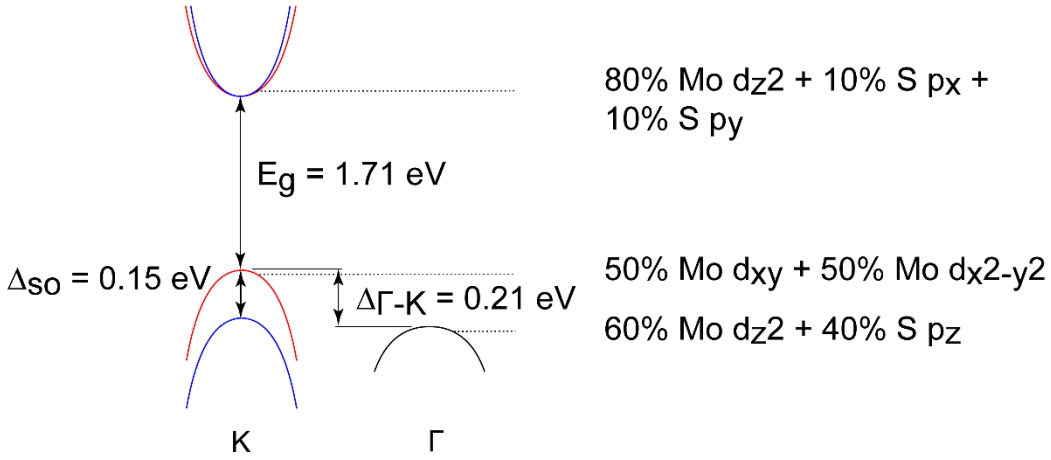
Bulk MoS_2





Monolayer MoS_2

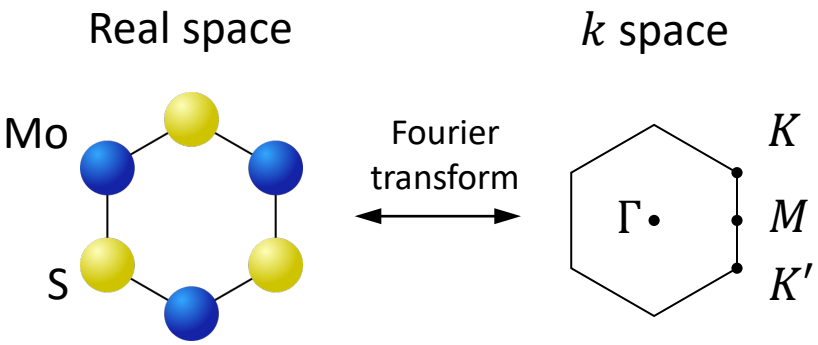


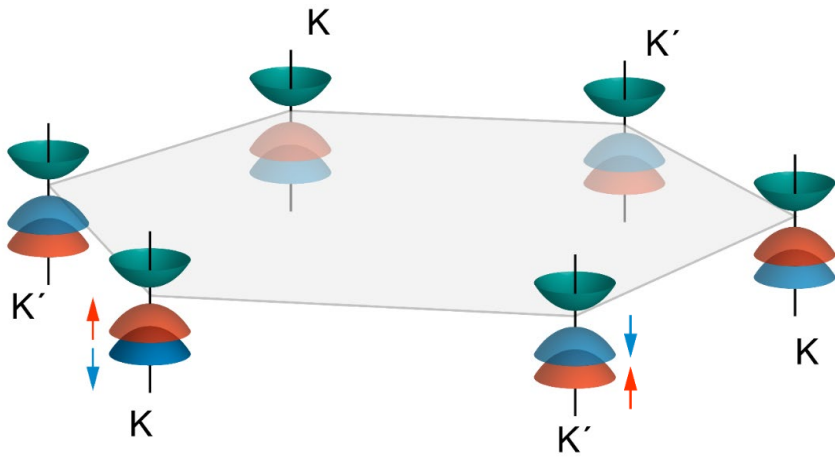


Kuc…Heine; Physical Review B (2011)

Yazyev and Kis; Materials Today (2014)

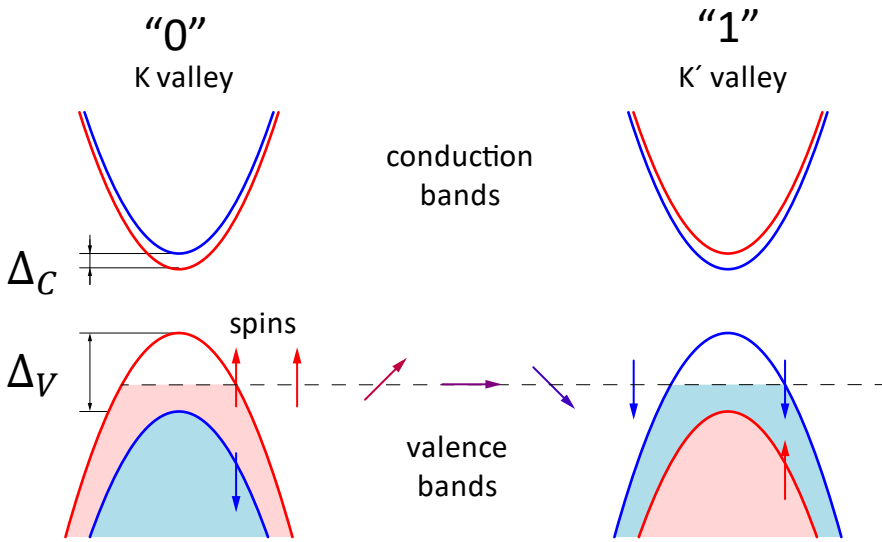
Valleytronics with TMDC (MX_2) Monolayers





K and K' not the same because of spin-orbit coupling

Xiao, Wang Yao et al., PRL (2012)

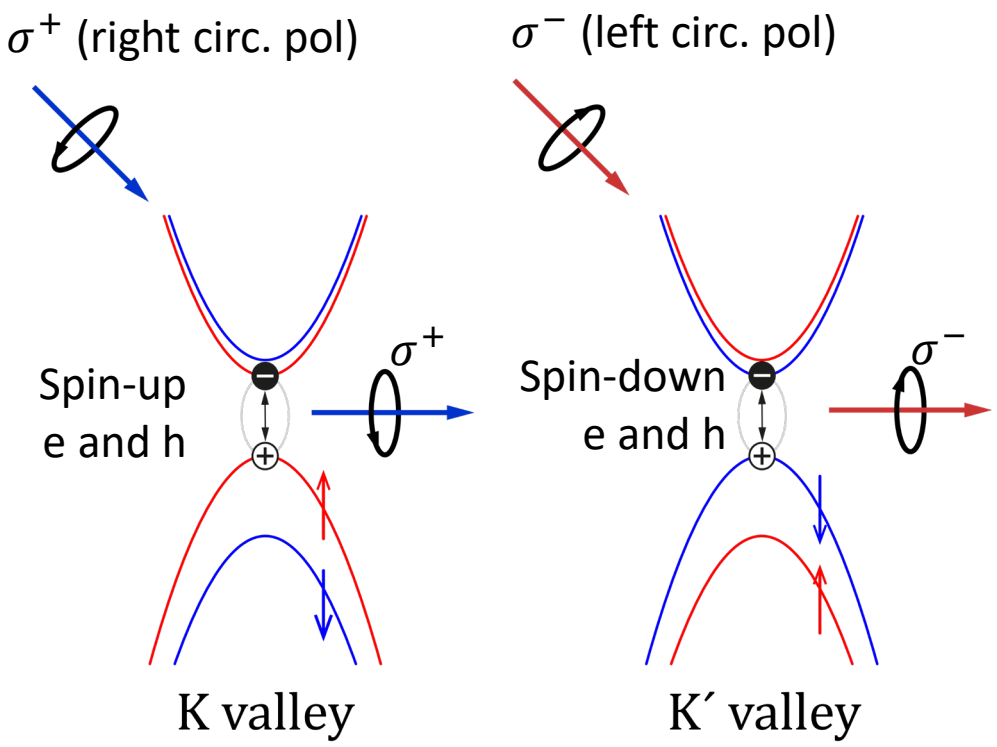


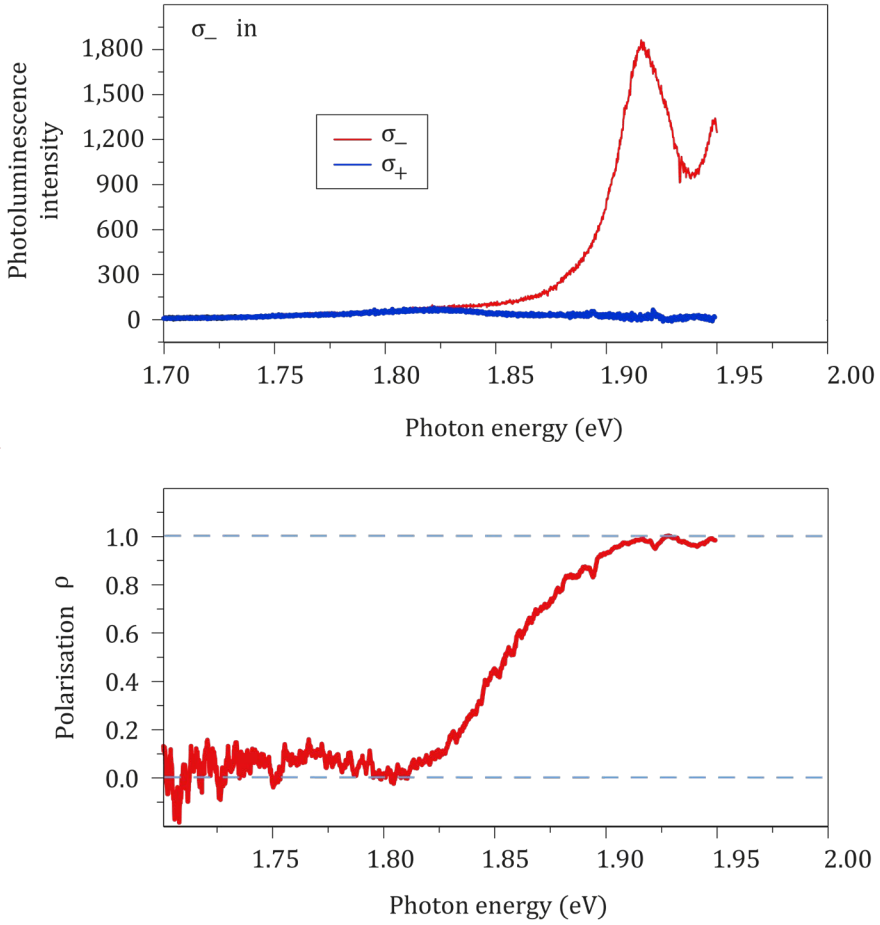
Material	Δ_V	Δ_C
MoS_2	148 meV	3 meV
$MoSe_2$	186 meV	22 meV
WS_2	430 meV	−32 meV
WSe_2	460 meV	−37 meV

Ochoa et al.; Phys. Rev. B (2014)

How do we Select and Detect the Valleys?

Simplest approach: circular dichroism

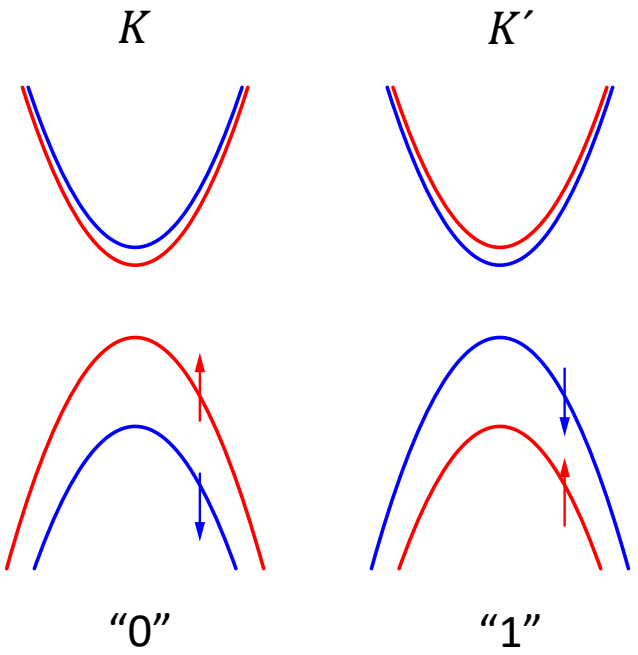




Zeng et al. Nature Nanotech. (2012)
Mak et al. Nature Nanotech. (2012)
Cao et al. Nature Nanotech (2012)

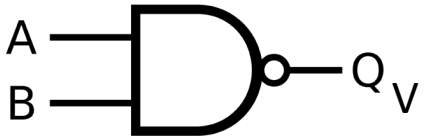
Valleytronics with TMDC (MX_2) Monolayers

Injection		Detection	
Light absorption	(σ^+, σ^-)	Light emission	(σ^+, σ^-)
Spin injection	↑, ↓	Light emission	(σ^+, σ^-)
Light absorption	(σ^+, σ^-)	Spin detection	↑, ↓
Spin injection	↑, ↓	Spin detection	↑, ↓



Valleytronics for reversible computing

Valley version of the NAND gate:



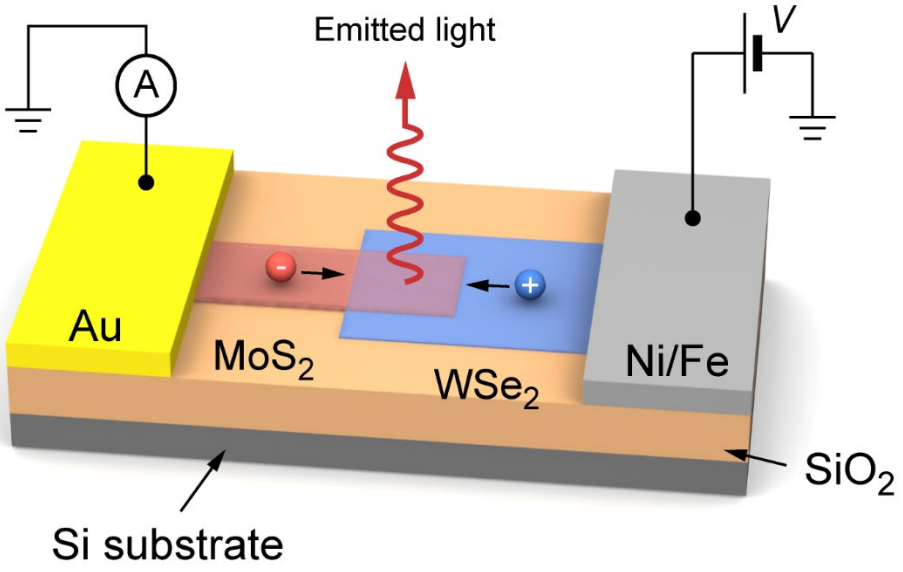
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

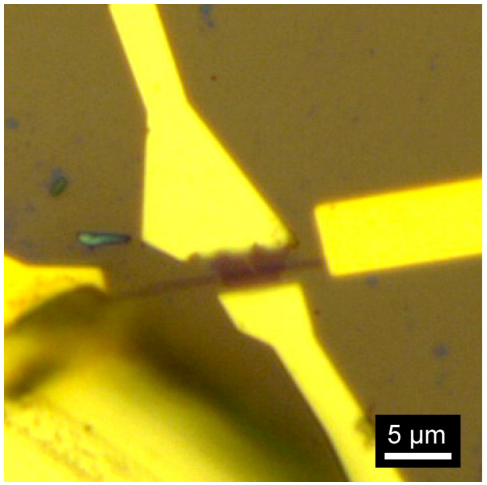
"colored" by the valley state

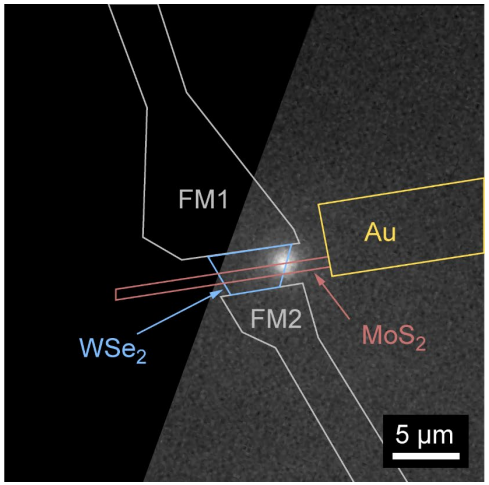
Ang et al. Phys. Rev. B (2017)

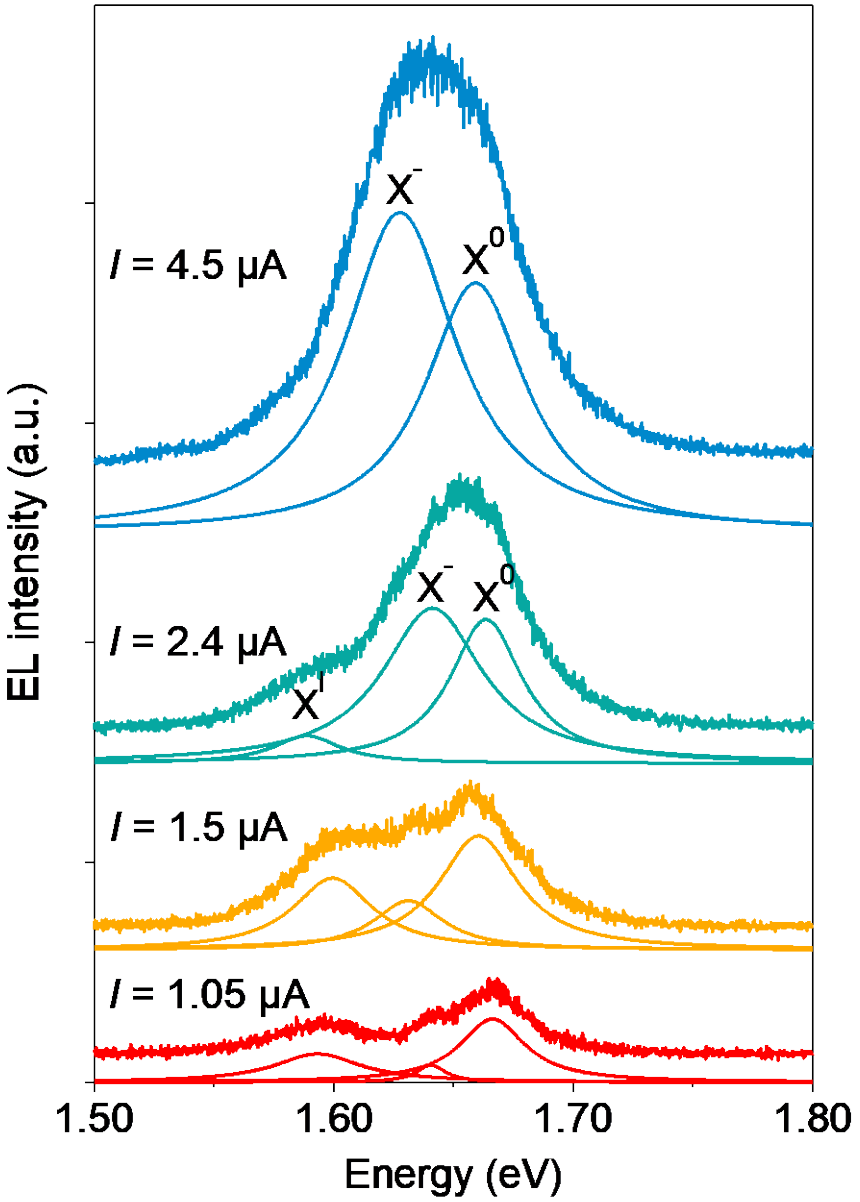
Use the valley states (polarized K, unpolarized, polarized K') to distinguish the three outcomes and achieve reversibility

Valley/spin IN – Light OUT



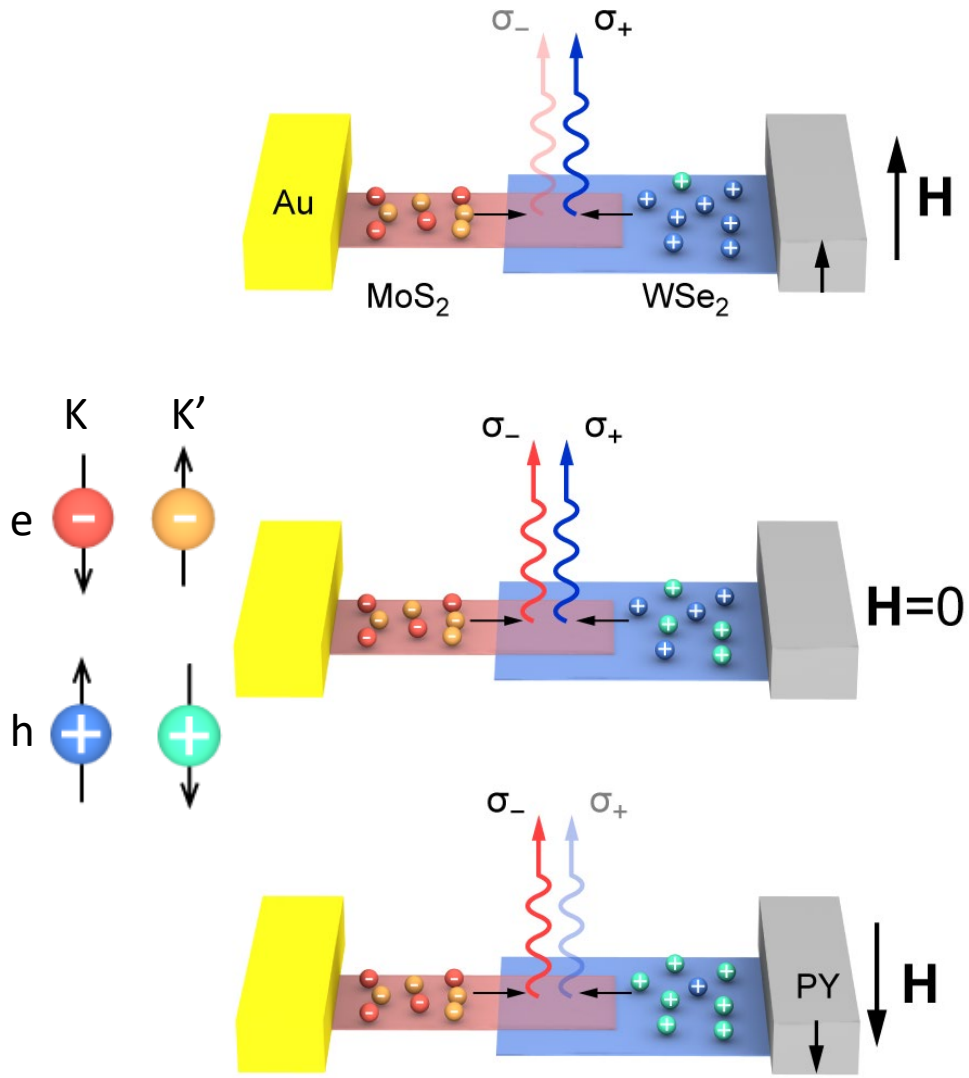


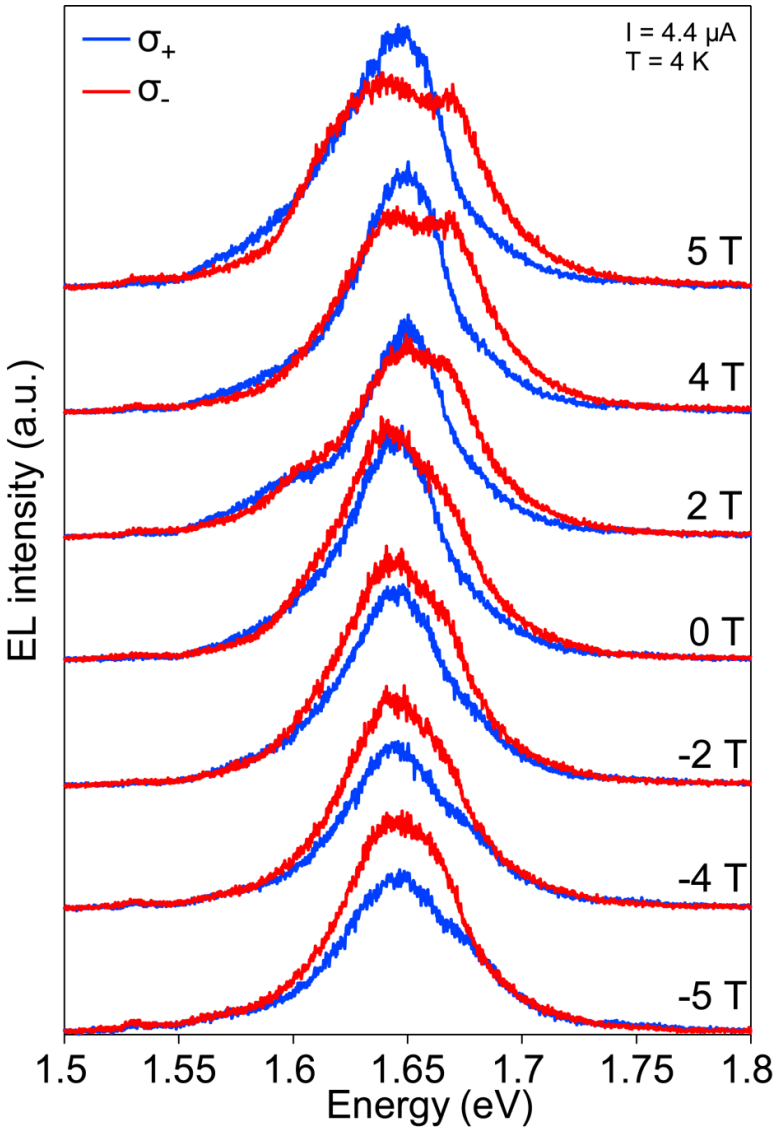




Lopez Sanchez…Kis; Nano Lett. (2016)

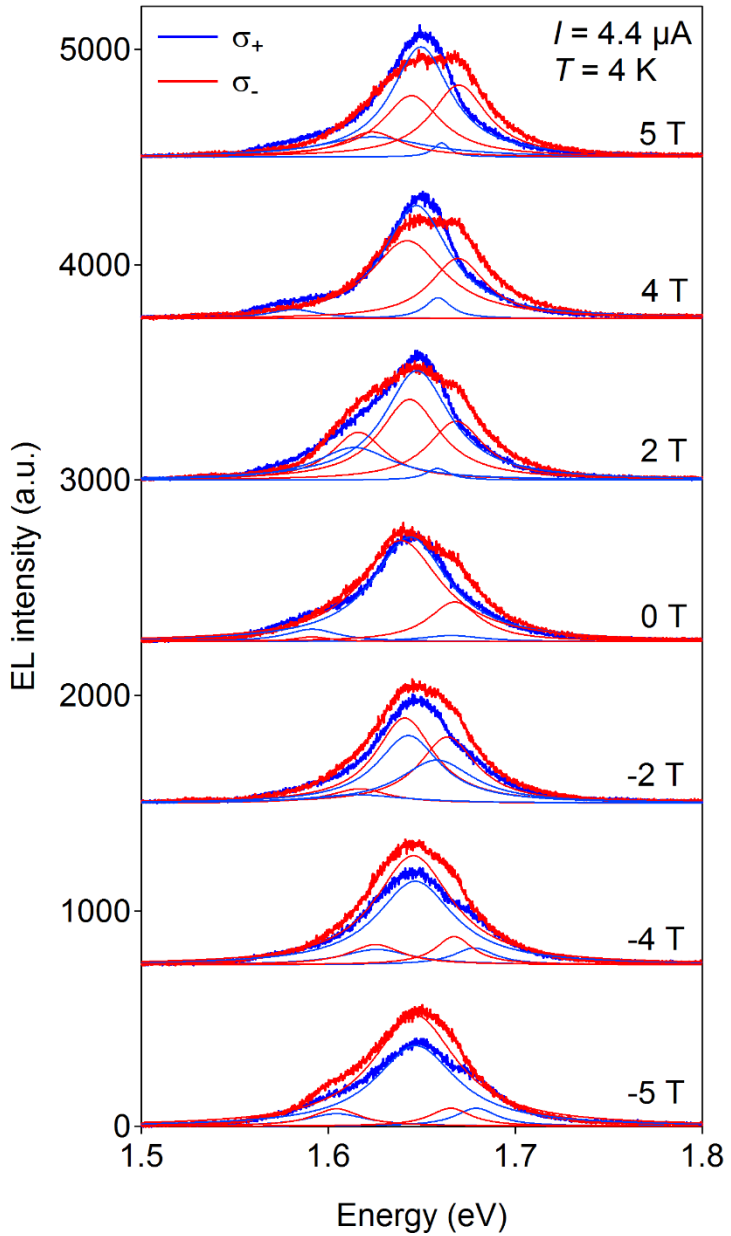
Valley polarization by spin injection



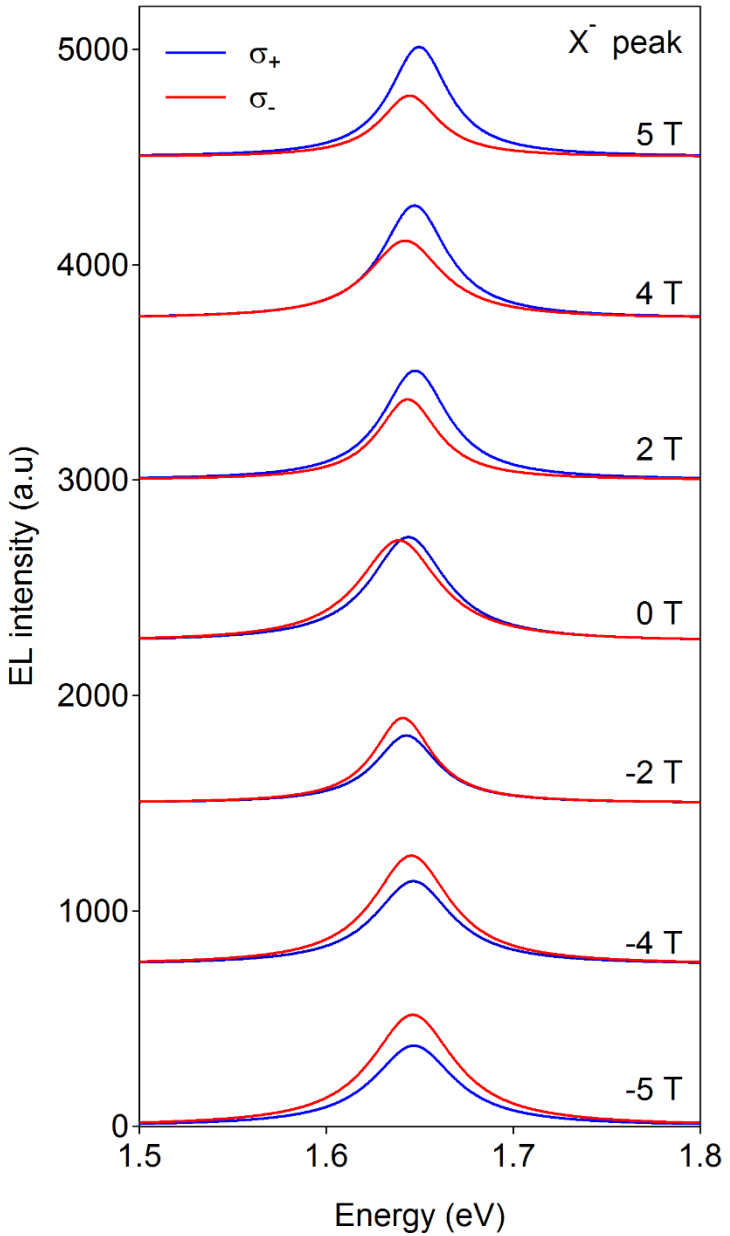


Lopez Sanchez…Kis; Nano Lett. (2016)

Valley Polarization by Spin Injection

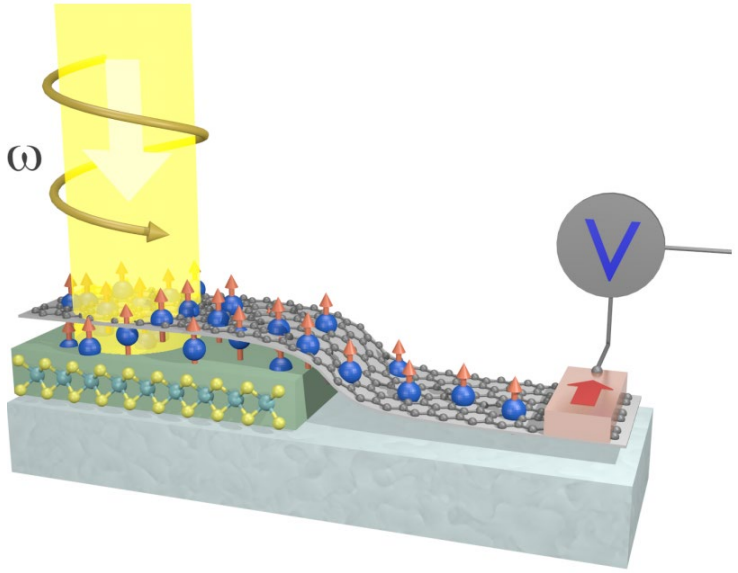


Lorentzian fits, X^- exciton



Optical spin injection (Light IN – Valley/spin OUT)

Theoretical proposal



Gmitra and Fabian; PRB (2015)

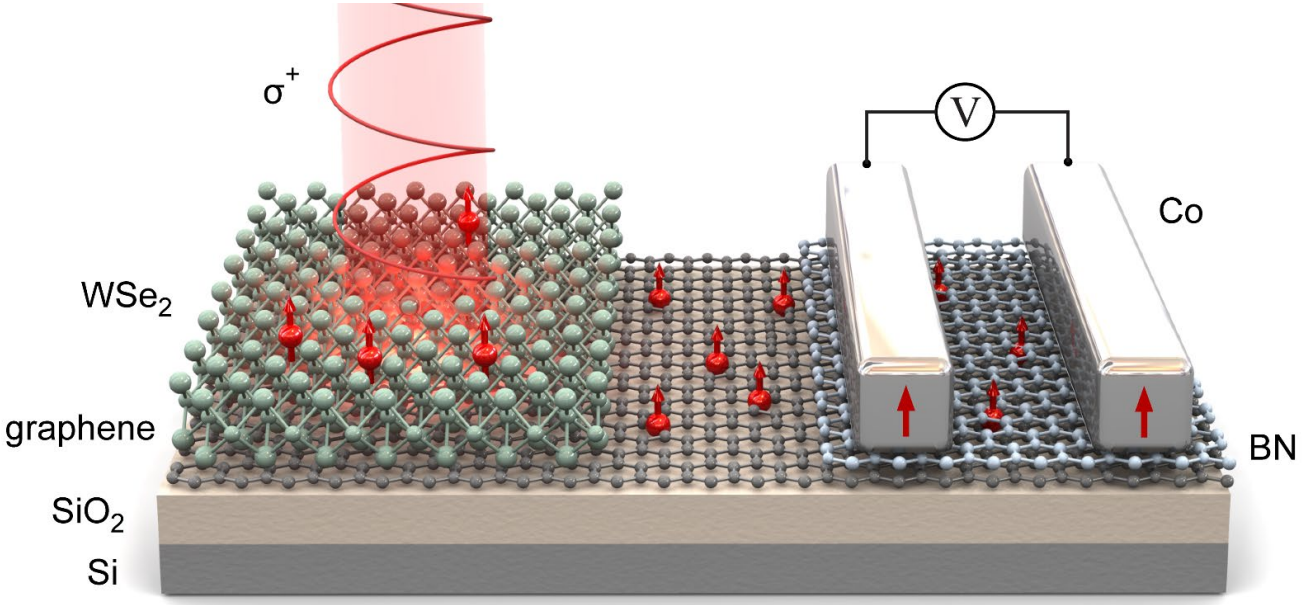
TMDC/Graphene
Van der Waals heterostructure

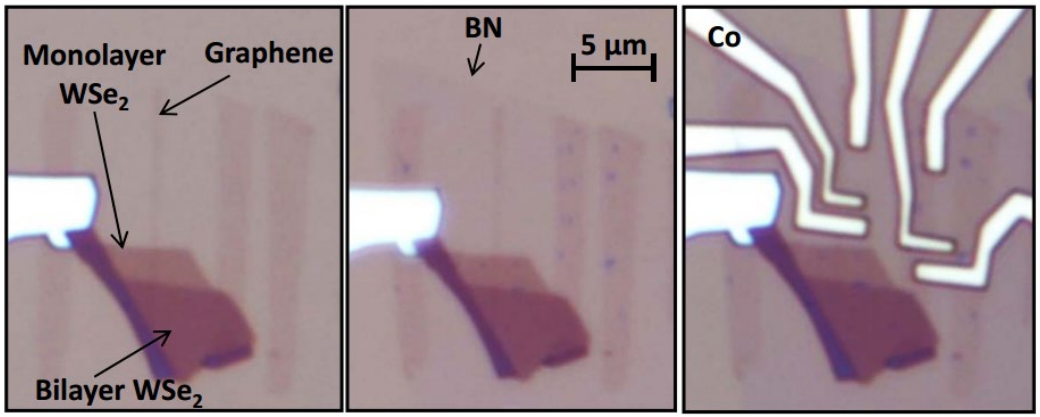
1. Valley addressed by circularly polarized light
2. Spin coupled to the excited valley
3. Spin diffuses into graphene
4. Spin transport inside the graphene channel
5. Nonlocal electrical detection

Optical spin injection (Light IN – Valley/spin OUT)

Avsar, Unuchek…Kis; ACS Nano (2017)

Proposed by: Gmitra and Fabian; PRB (2015)



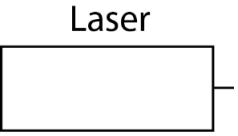


See also:

Luo…Kawakami; Nano Lett. (2017)

Experimental Scheme

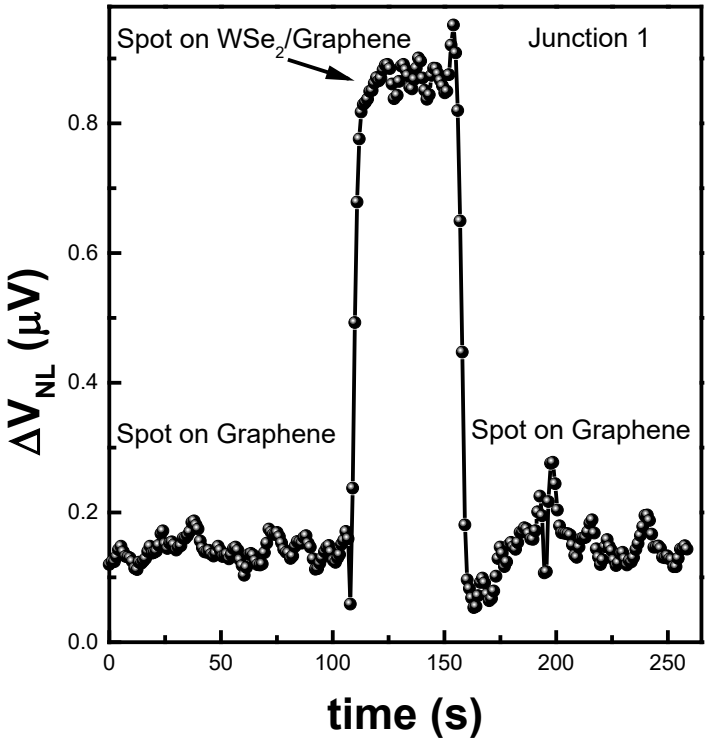
Main experiment
$\lambda/4$ modulation



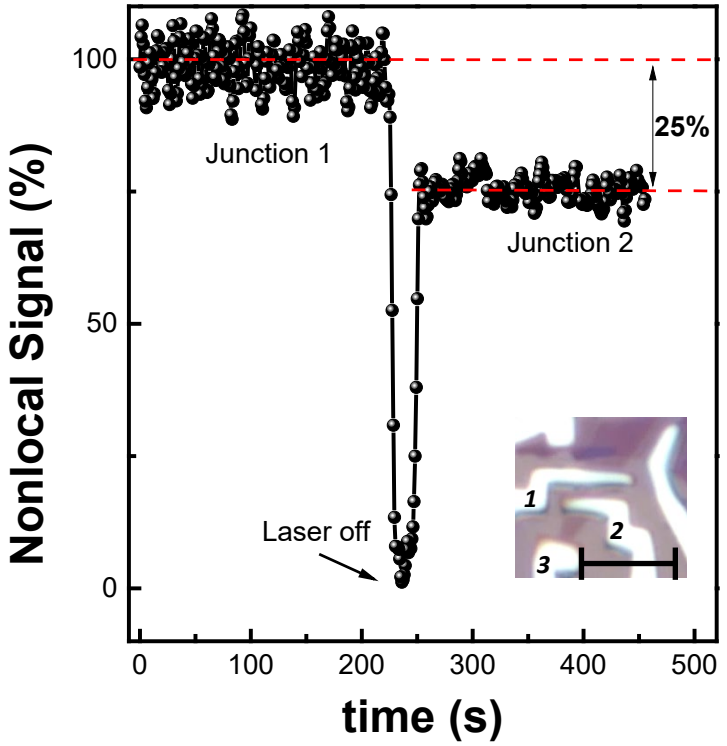
PEM + lock-in amplifier 1f

Detection of the Spin Signal

Signal on the heterostructure

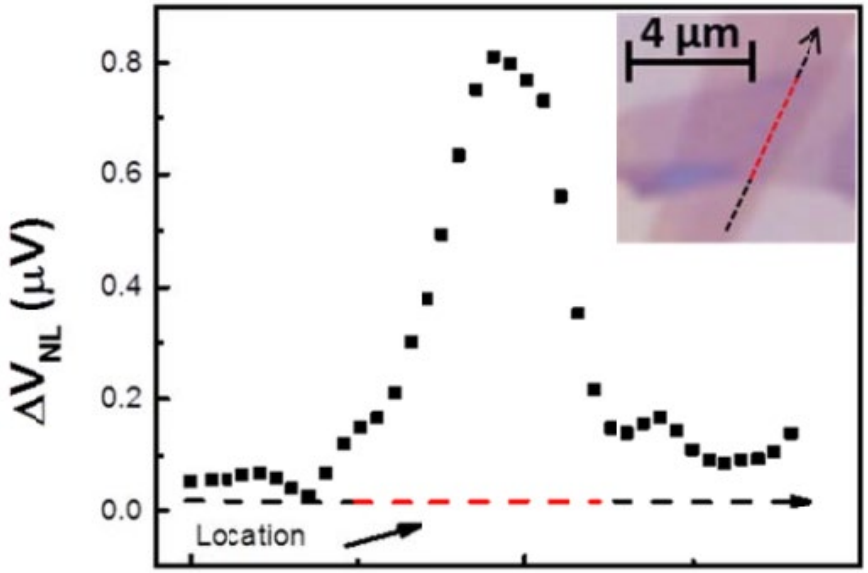


Signal attenuation

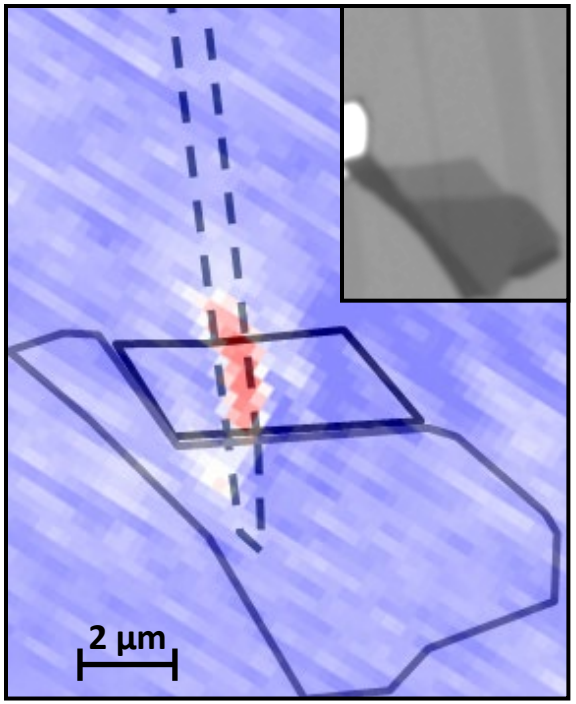


Spatial Dependence

Dev1 Resonant – 720nm



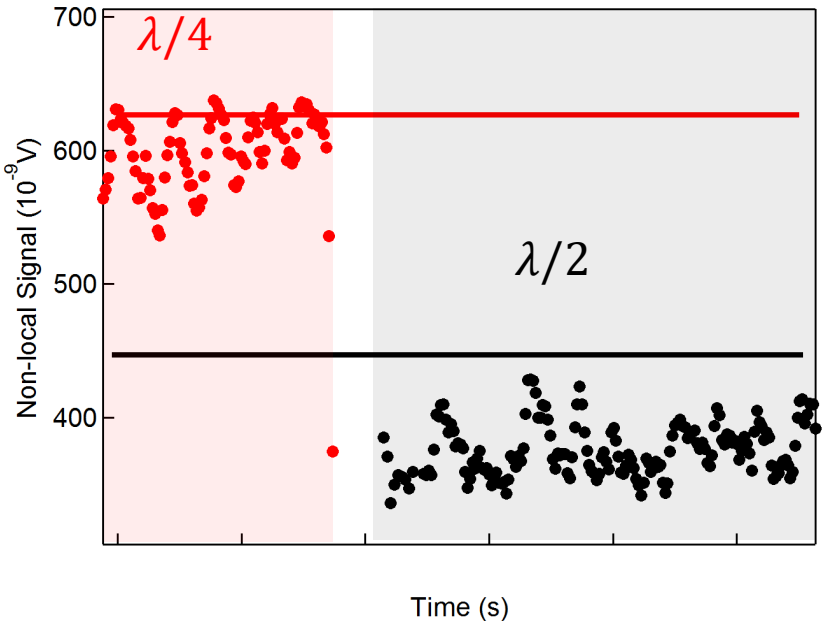
Dev2 647nm



Control Experiment

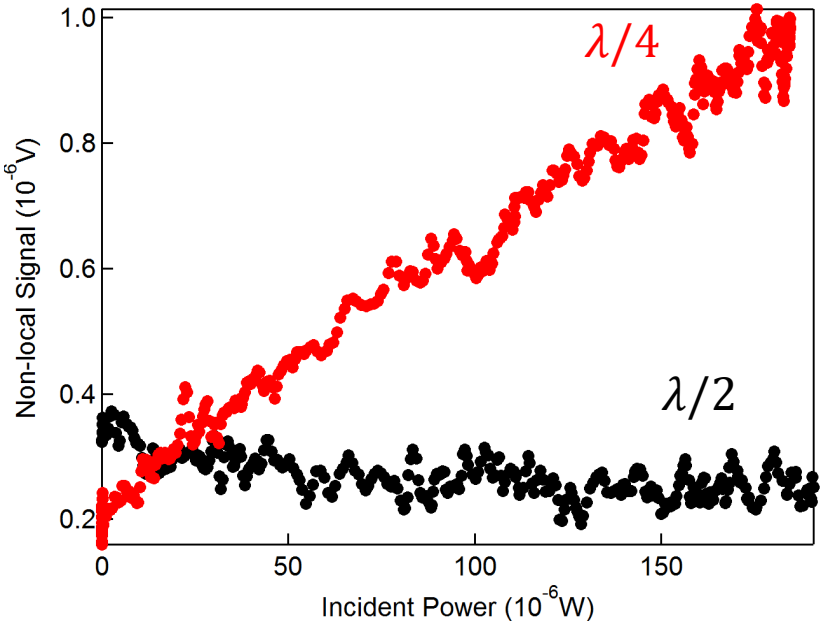
λ/2 modulation (linear polarization)

$\lambda/4$-> $\lambda/2$ modulation



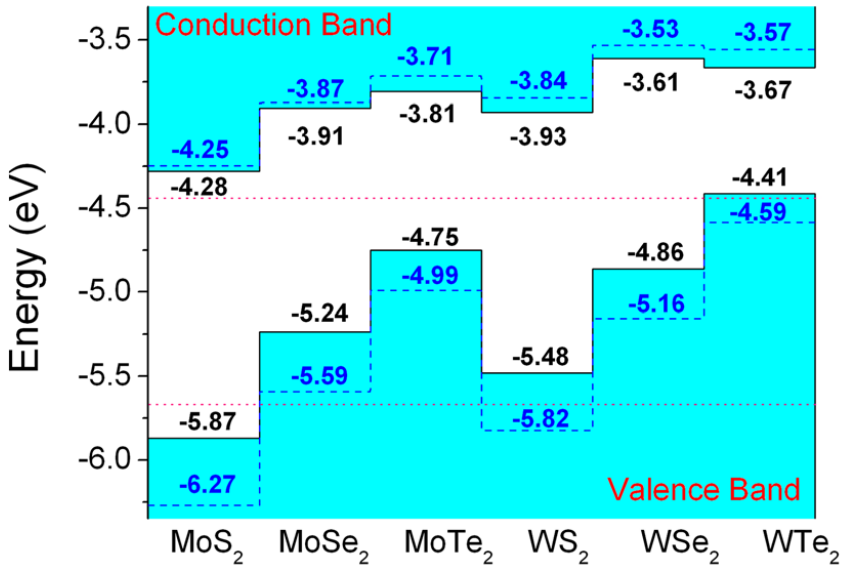
- $\lambda/4$ – original signal
- $\lambda/2$ – noise floor

Power dependence

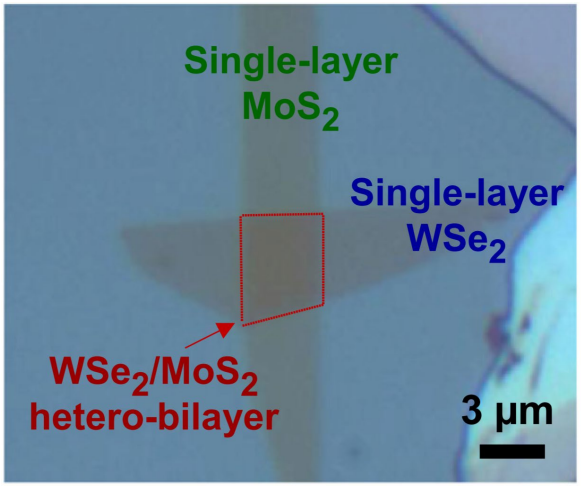


- $\lambda/4$ – linear
- $\lambda/2$ – no dependence

Interlayer Excitons in TMDCs

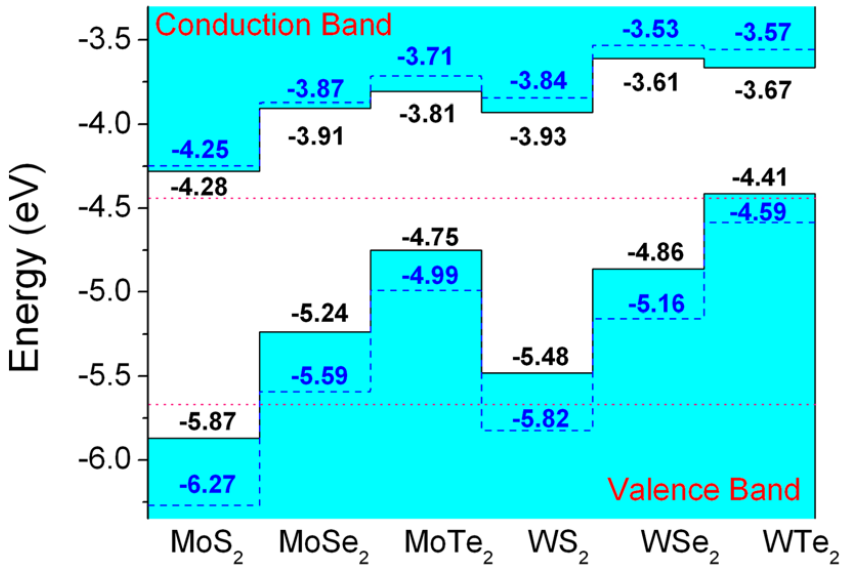


Kang, Jun, et al, APL (2013)



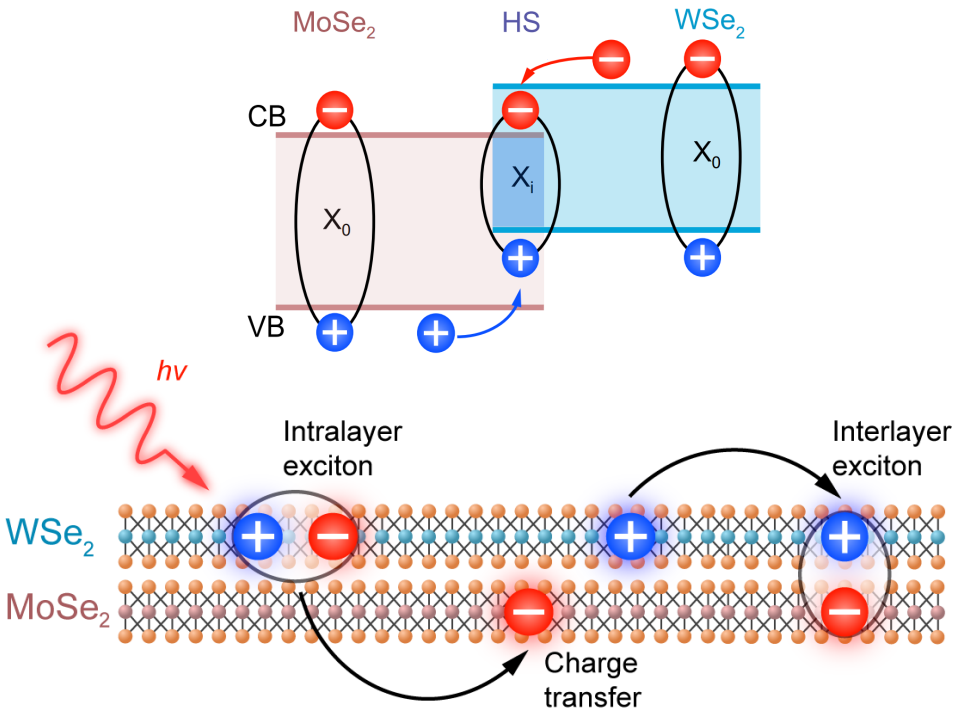
Fang…Javey; PNAS (2014)

Interlayer Excitons in TMDCs

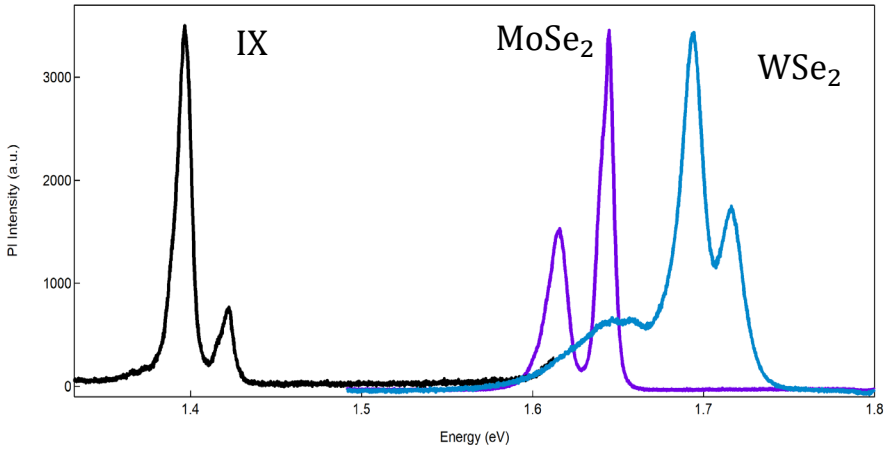


Kang, Jun, et al, APL (2013)

Band Diagram



Photoluminesce spectra



Spatial separation of charges:

- Built-in dipole moment -> manipulation
- Long lifetime ~ ns
- Large binding energy ~ 100s of meV

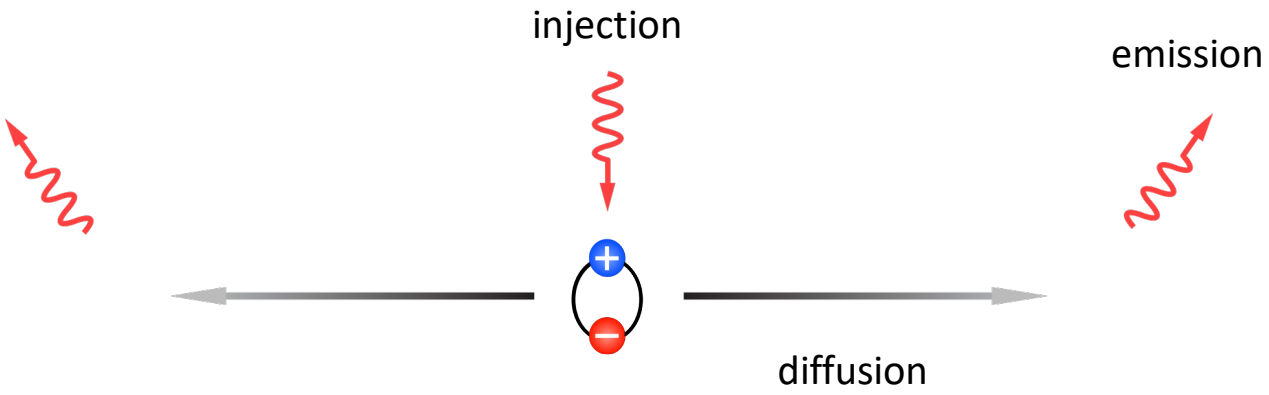
Related work:

Fang et al, PNAS (2014)
P. Rivera, et al. *N. Com* (2015)
P. Rivera, et al. *Science*(2016)
Hanbicki, et al. *ACS Nano* (2016)

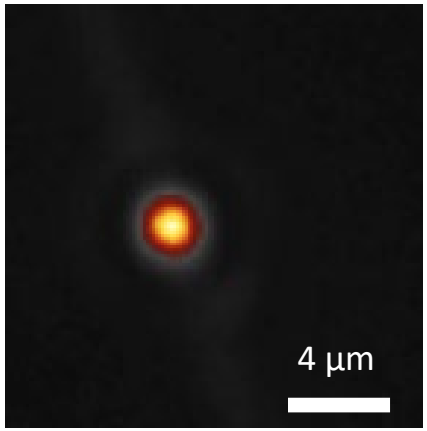
Exciton Manipulation in a Device

Exciton diffusion

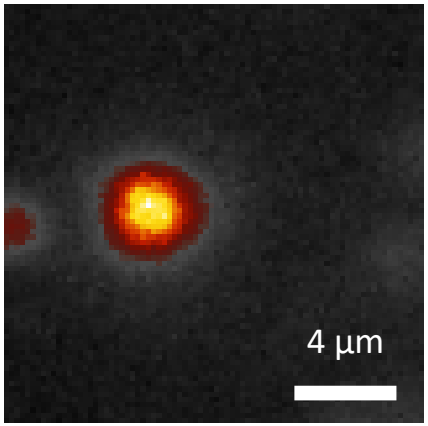
Driving forces: $\nabla T, \nabla \mu$



Excitation spot



IX emission

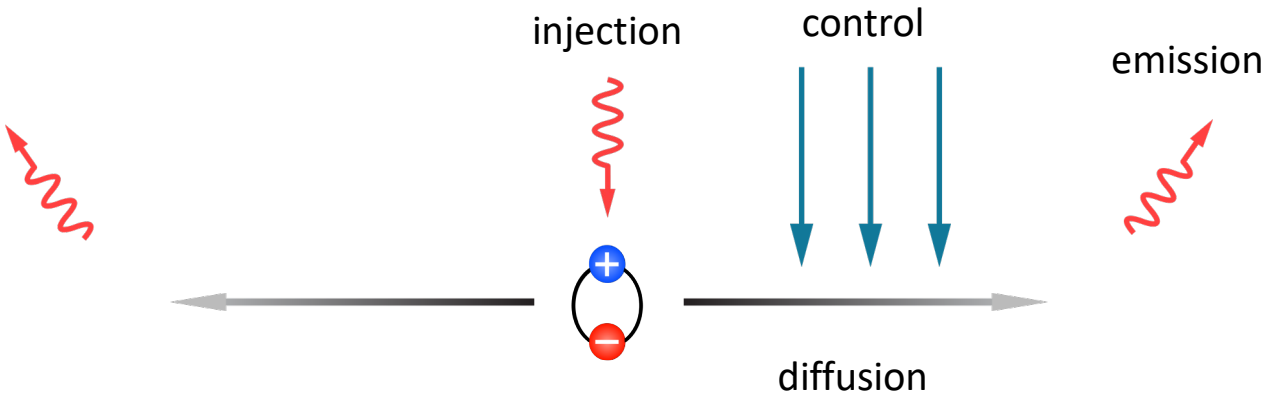


7 – 740 µW

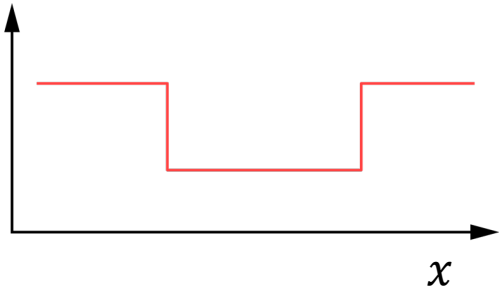
Exciton Manipulation in a Device

Exciton diffusion

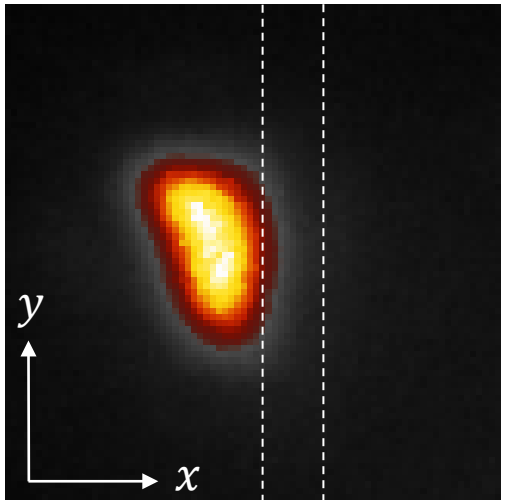
Driving forces: $\nabla T, \nabla \mu$

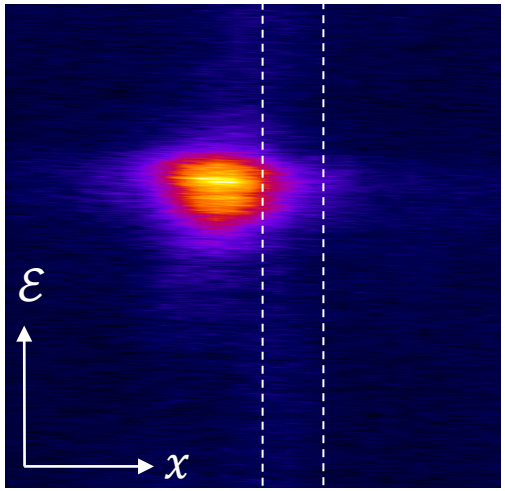


$$\varphi_{el} = \delta E = -p_z E_z(x, y)$$



IX emission





Simplest device:

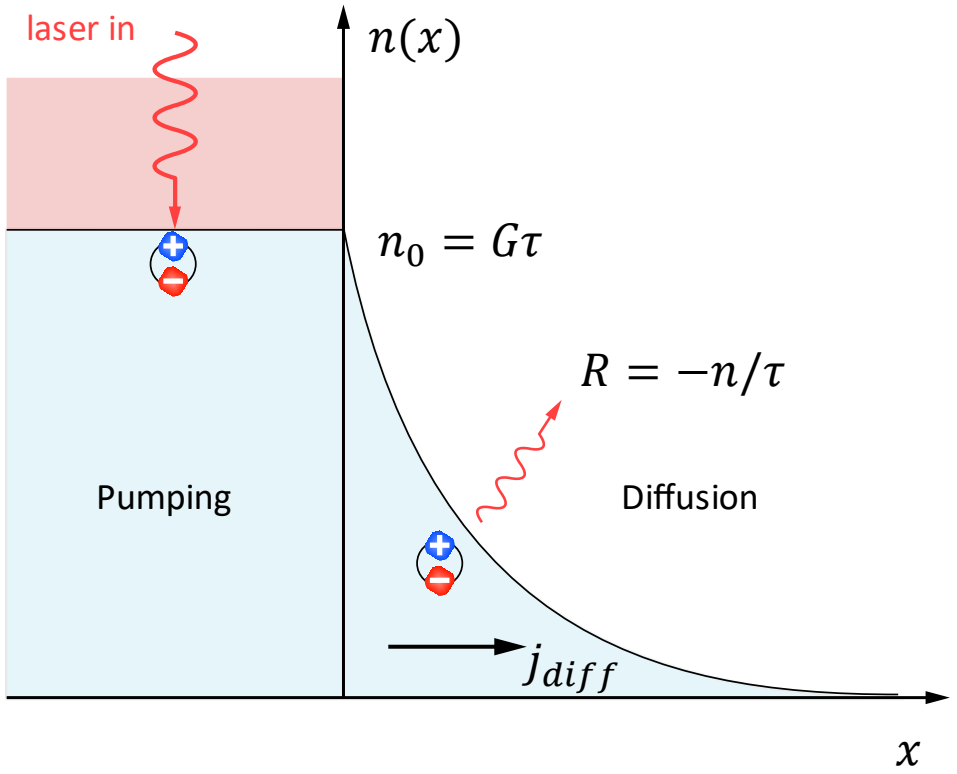
Excitonic transistor/switch

Exciton manipulation in a device

Exciton diffusion governed by diffusion equation with an external potential:

$$D\frac{\partial^2 n}{\partial x^2} - \frac{D}{k_B T}\frac{\partial}{\partial x}\left(\frac{\partial \varphi}{\partial x} n\right) + G - \frac{n}{\tau} = \frac{\partial n}{\partial t}$$

$$\varphi_{el} = \delta E = -p_z E_z(x, y)$$

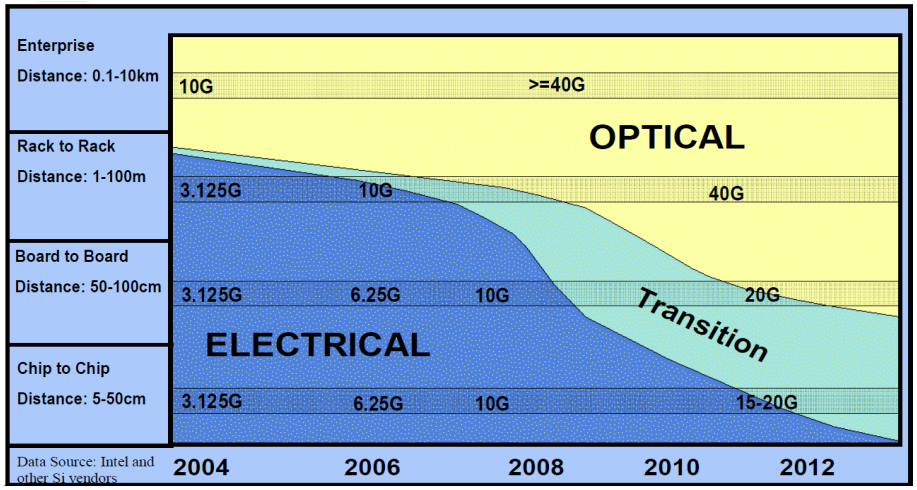


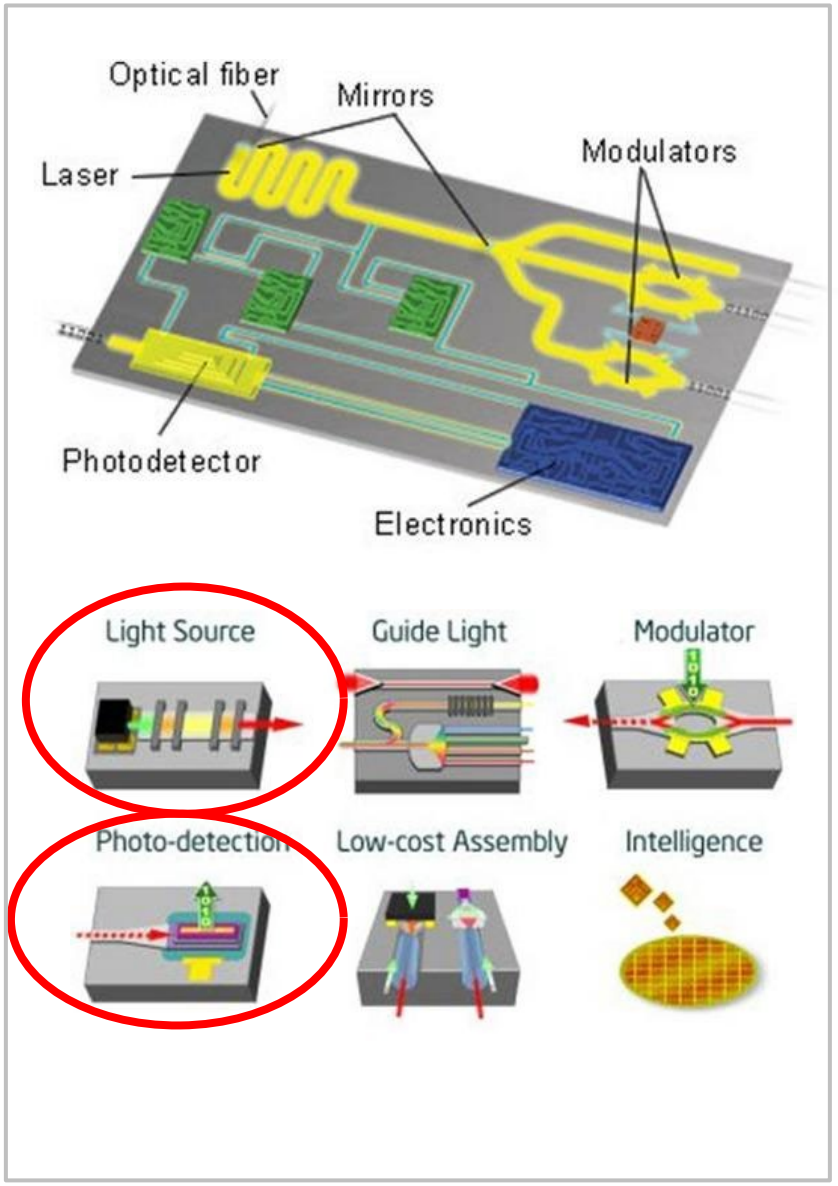
j_{diff}	current
n	exciton concentration
D	diffusion coefficient
τ	exciton lifetime
G	generation rate
R	recombination rate
p	dipole moment
φ	exciton potential
k_B	Boltzmann constant

Unuchek, Ciarrocchi et al. Nature (2018)

Ch 2.4: Optoelectronics and IT devices

Data load

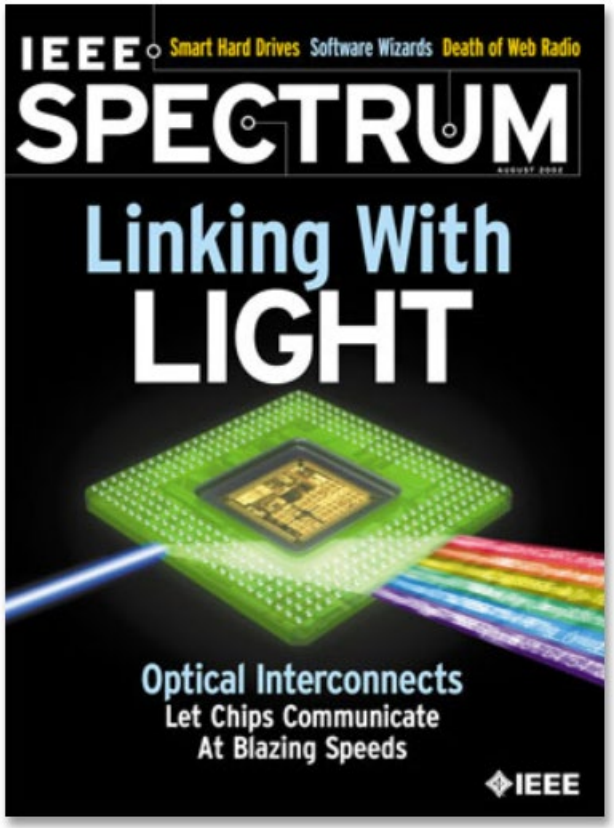




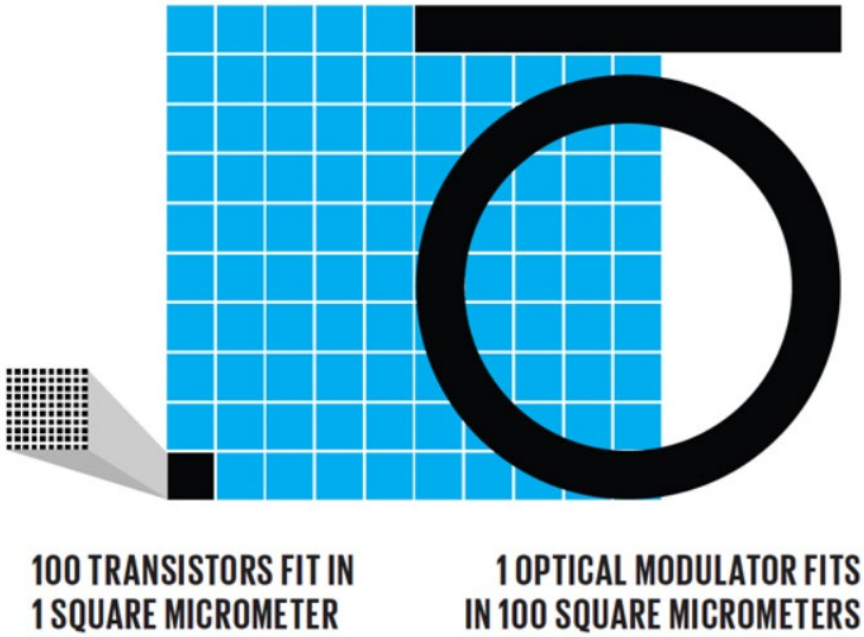
Flexible devices

From the TV show Westworld

Excitonic Devices



Savage; IEEE Spectrum (2002)



Levi; IEEE Spectrum (2018)

$$device\ size \gg particle\ size$$

$$photons: \lambda$$
$$excitons: Bohr\ radius$$

Excitonic transistors with III-V materials

AlAs/GaAs coupled quantum wells

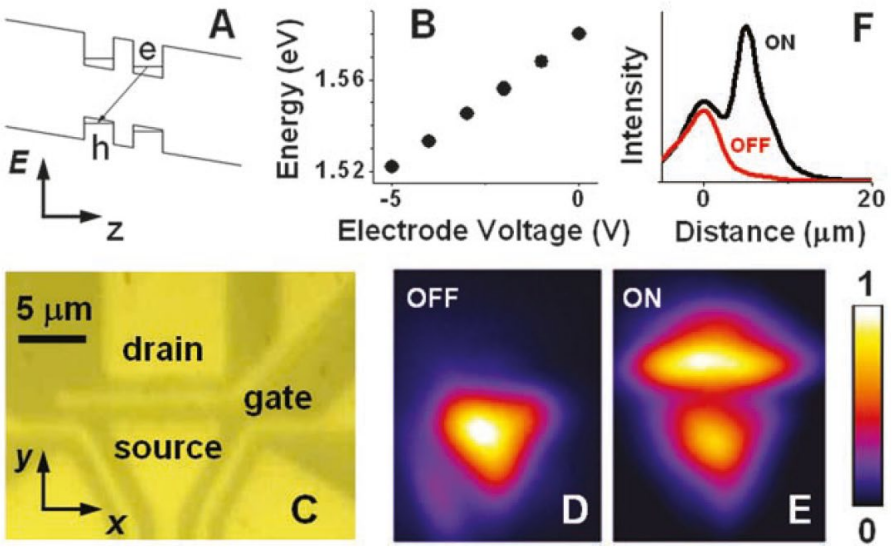
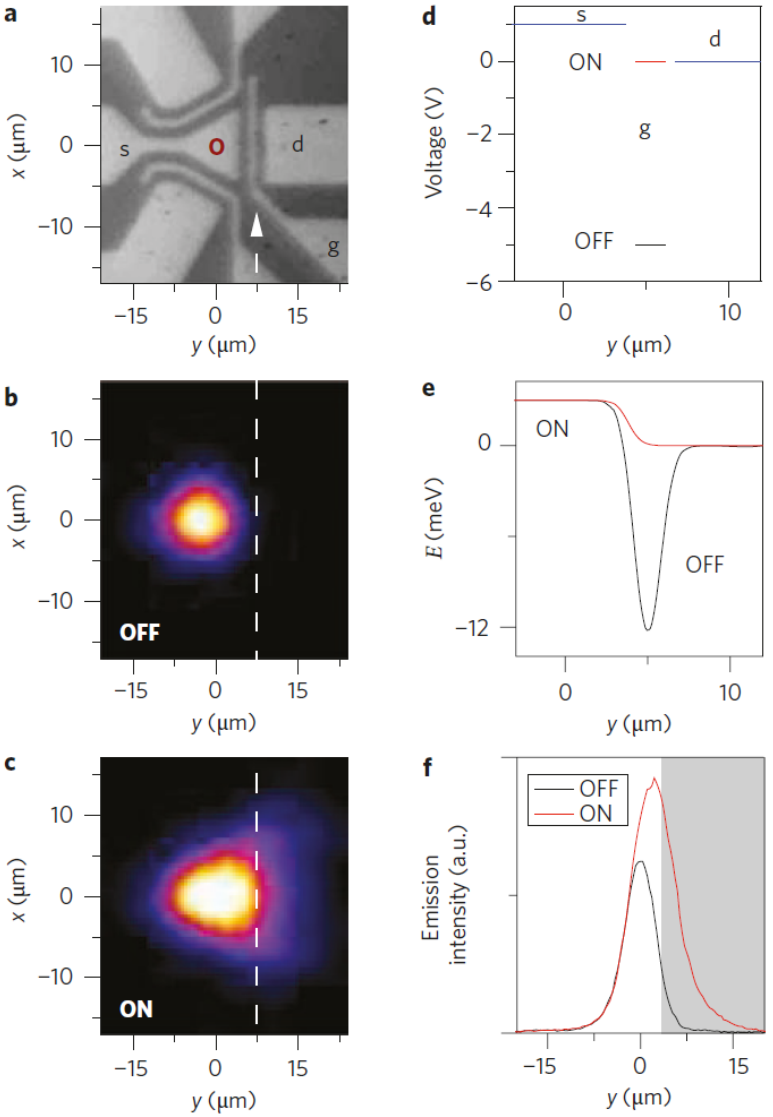
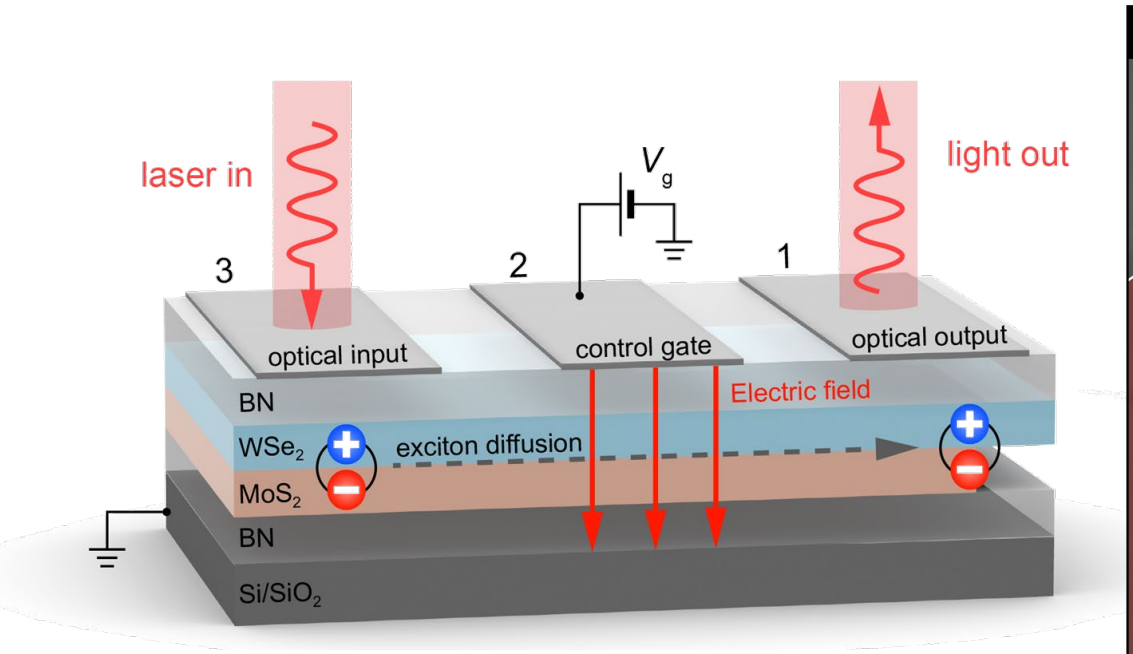


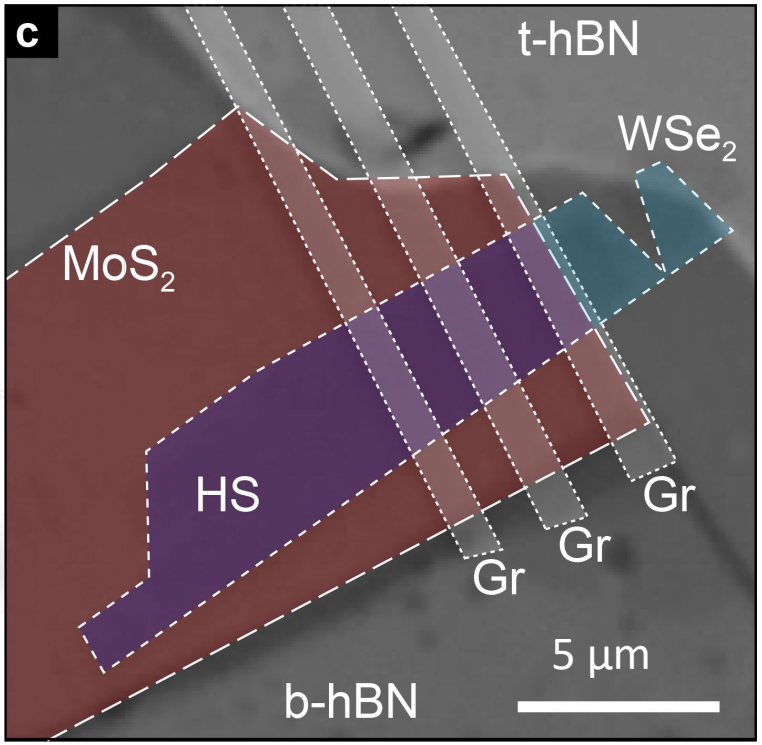
Fig. 1. Principle and operation of the EXOT. (**A**) Energy-band diagram of the CQW structure. e, electron; h, hole. (**B**) Control of the energy of the indirect excitons by gate voltage. (**C** to **E**) Realization of the EXOT. (C) Electrode pattern. [(D) and (E)] Emission of the EXOT in off (D) and on (E) states. The excitons are excited in the source electrode. The energy gradient for the indirect excitons from the source toward the drain is created by the electrode voltages $V_{source} = -1.5$ V and $V_{drain} = -2.5$ V. The exciton flux is controlled by the gate electrode: $V_{gate} = 0$ for the off state, and $V_{gate} = -3$ V for the on state. (**F**) Emission intensity along the exciton flux for off (red line) and on (black line) regimes [which correspond to the false-color images in (D) and (E)].



Grosso et al; Nature Phot. (2009)
Butov et al; Nature (2002)
High, Science (2008)

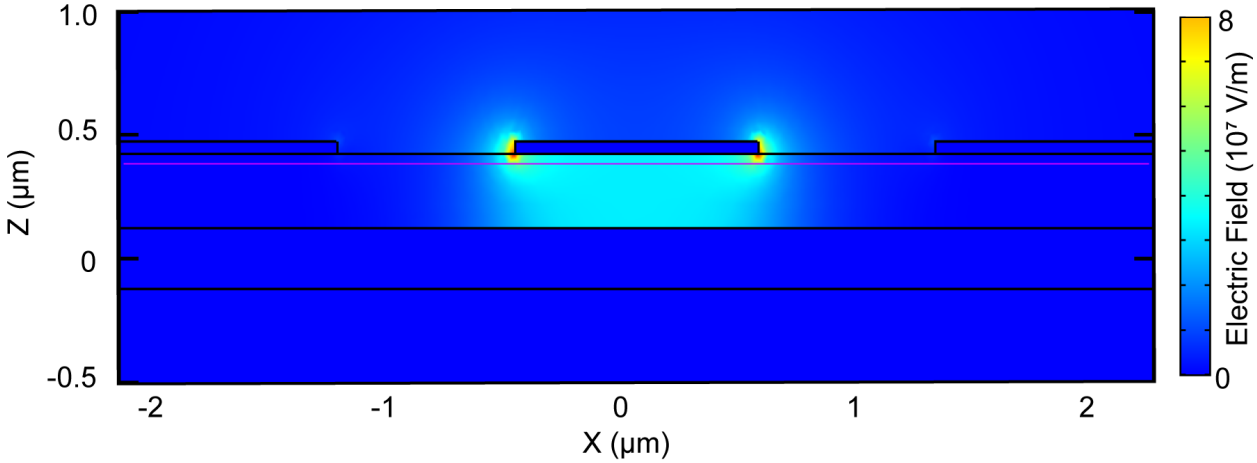
Room-temperature Excitonic Devices

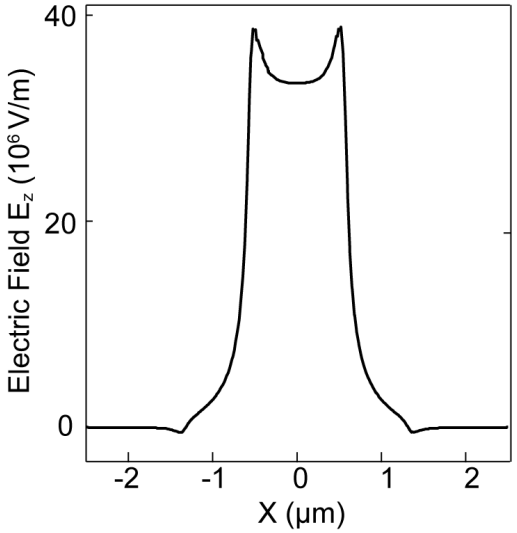


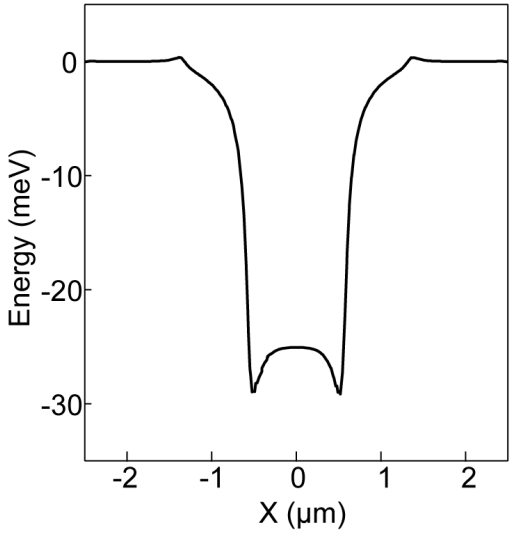


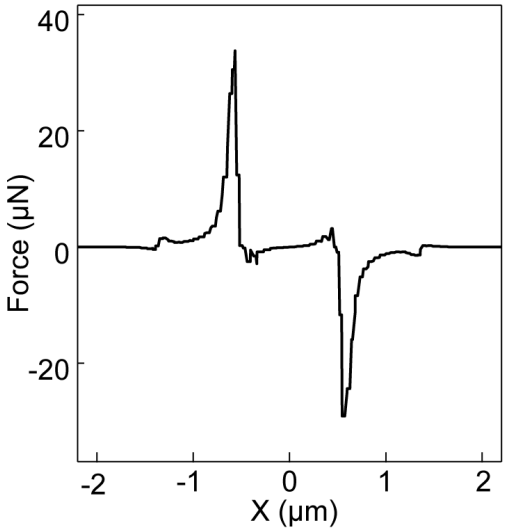
Unuchek, Ciarrocchi,…,Kis; Nature (2018)

Electric Field Simulations

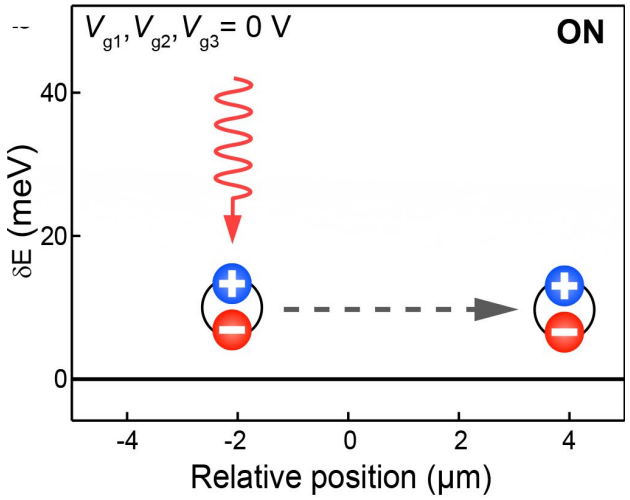


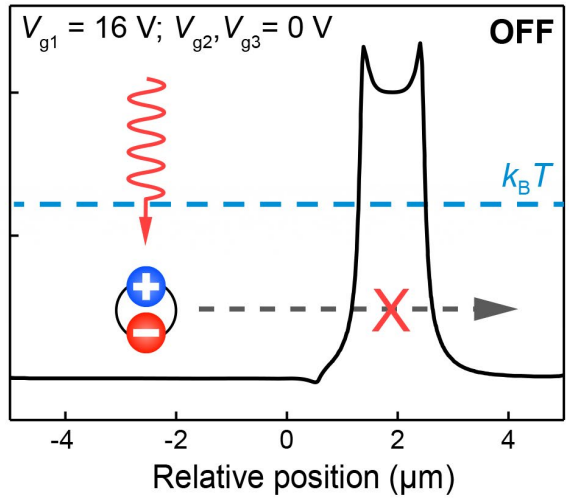


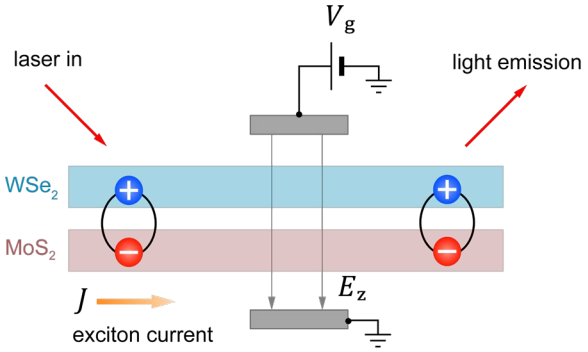


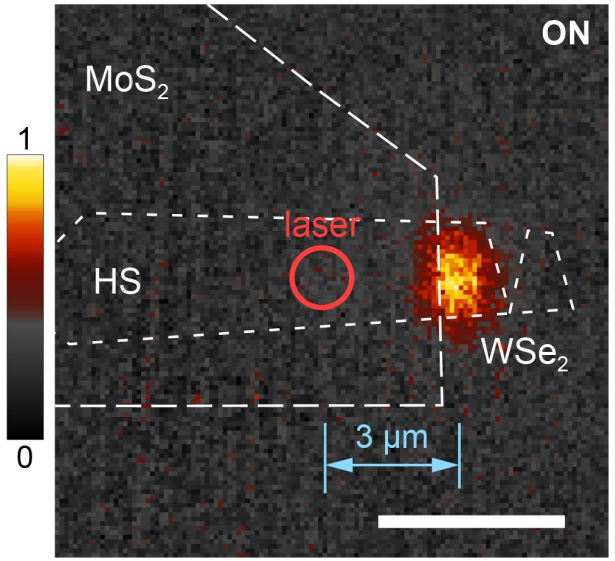


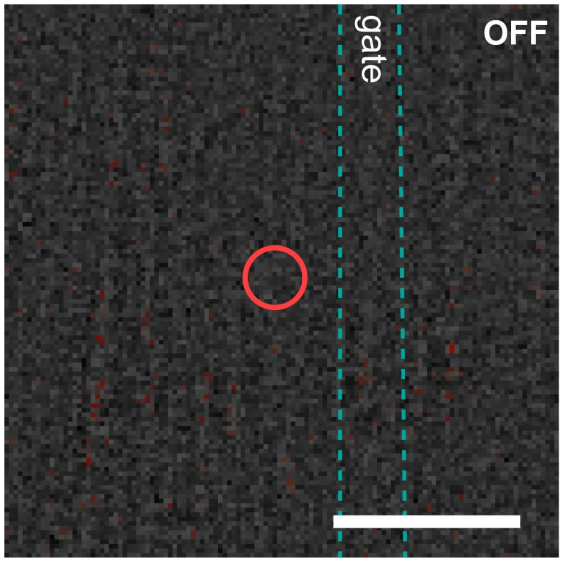
Gate Control: Switching





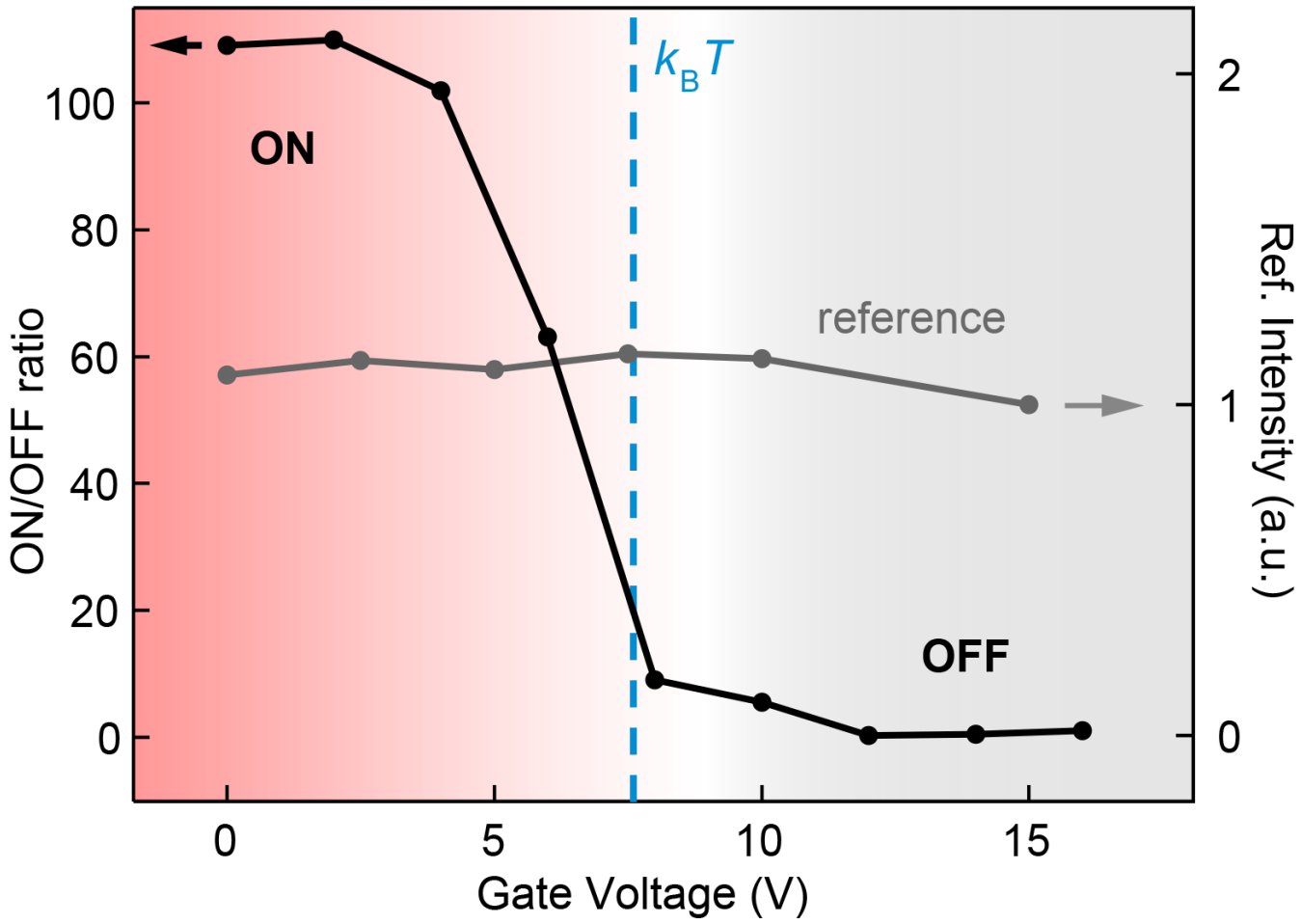




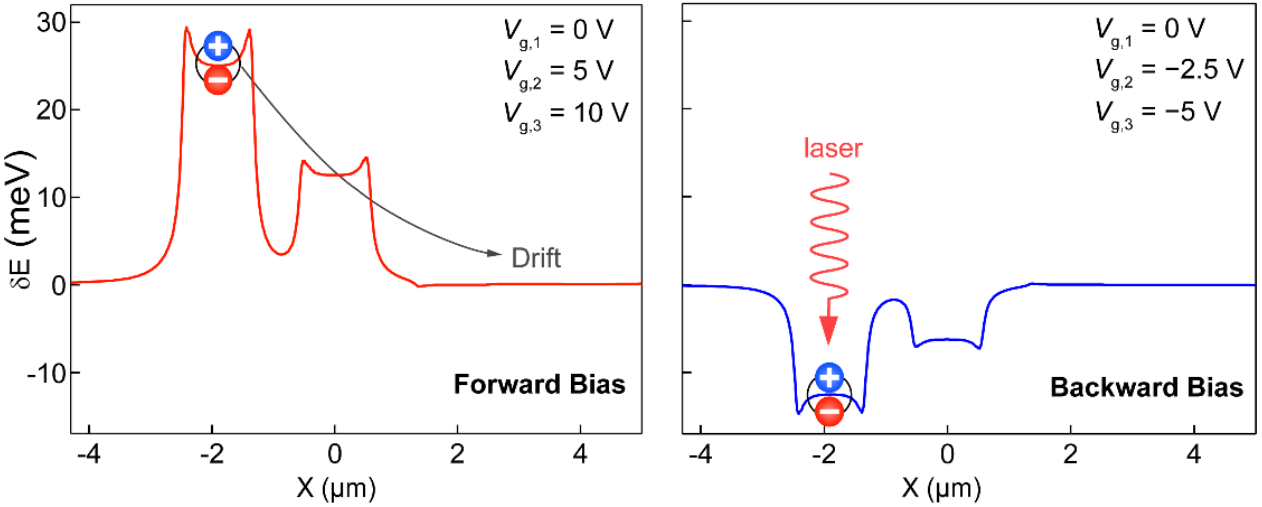


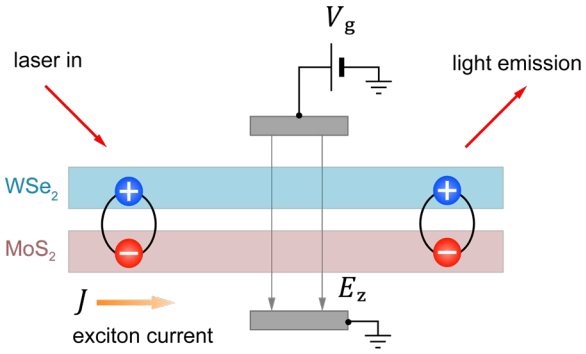
Unuchek, Ciarrocchi,…,Kis; Nature (2018)

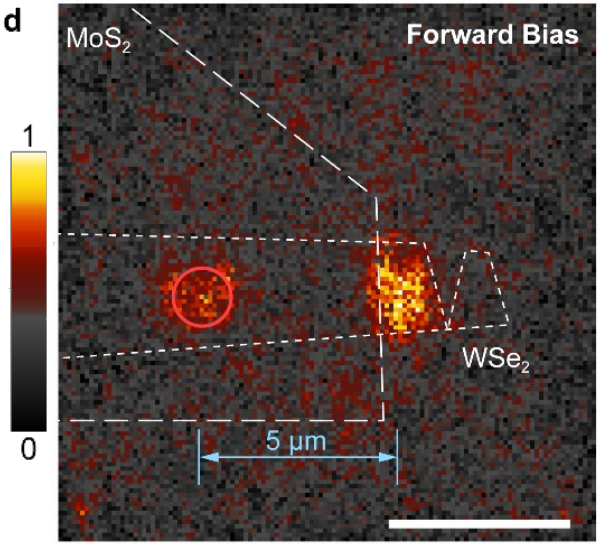
Gate Control: Switching

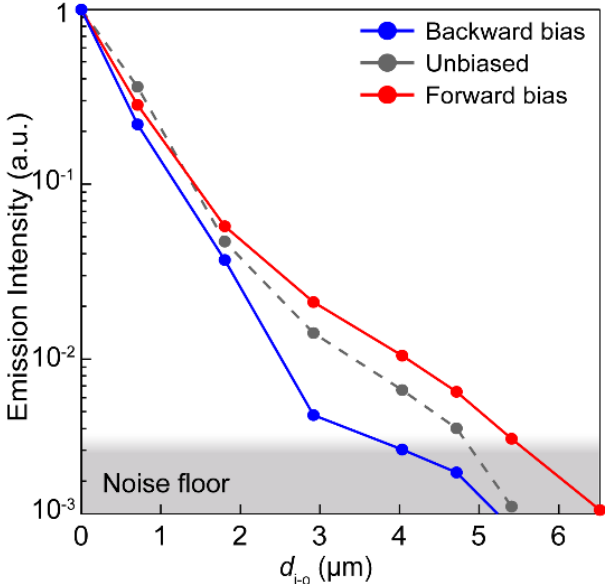


Gate Control: Enhanced Diffusion

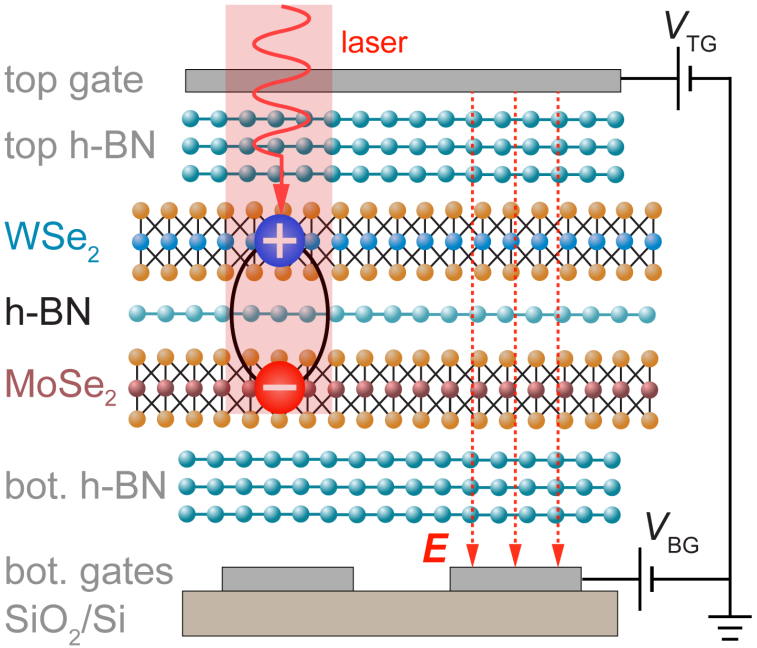


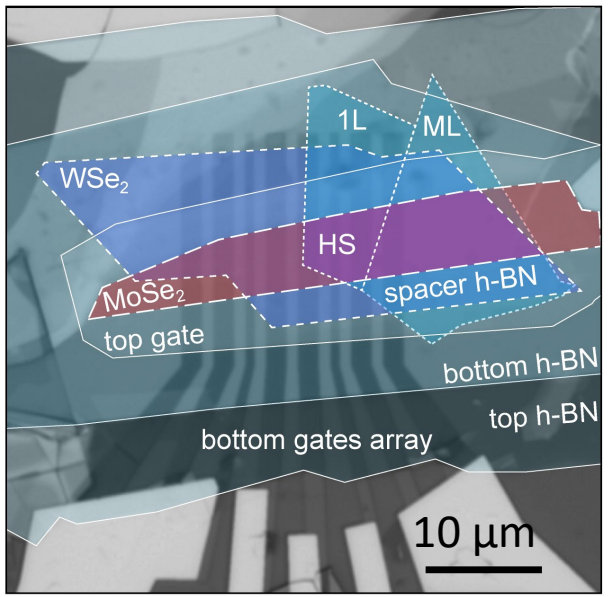


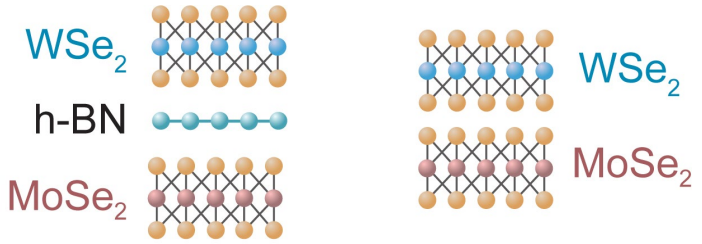


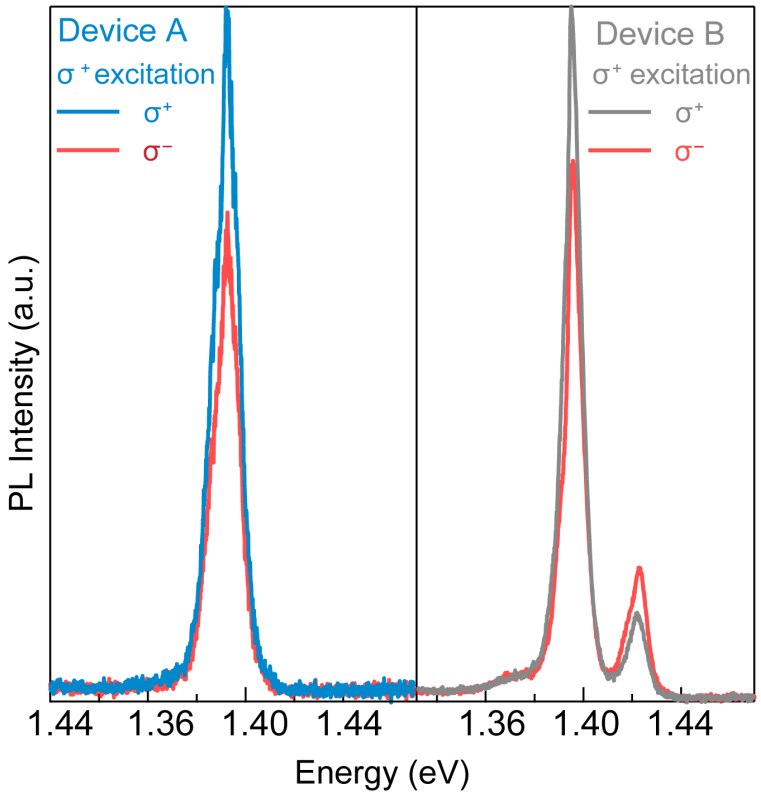


Engineered Interlayer Coupling







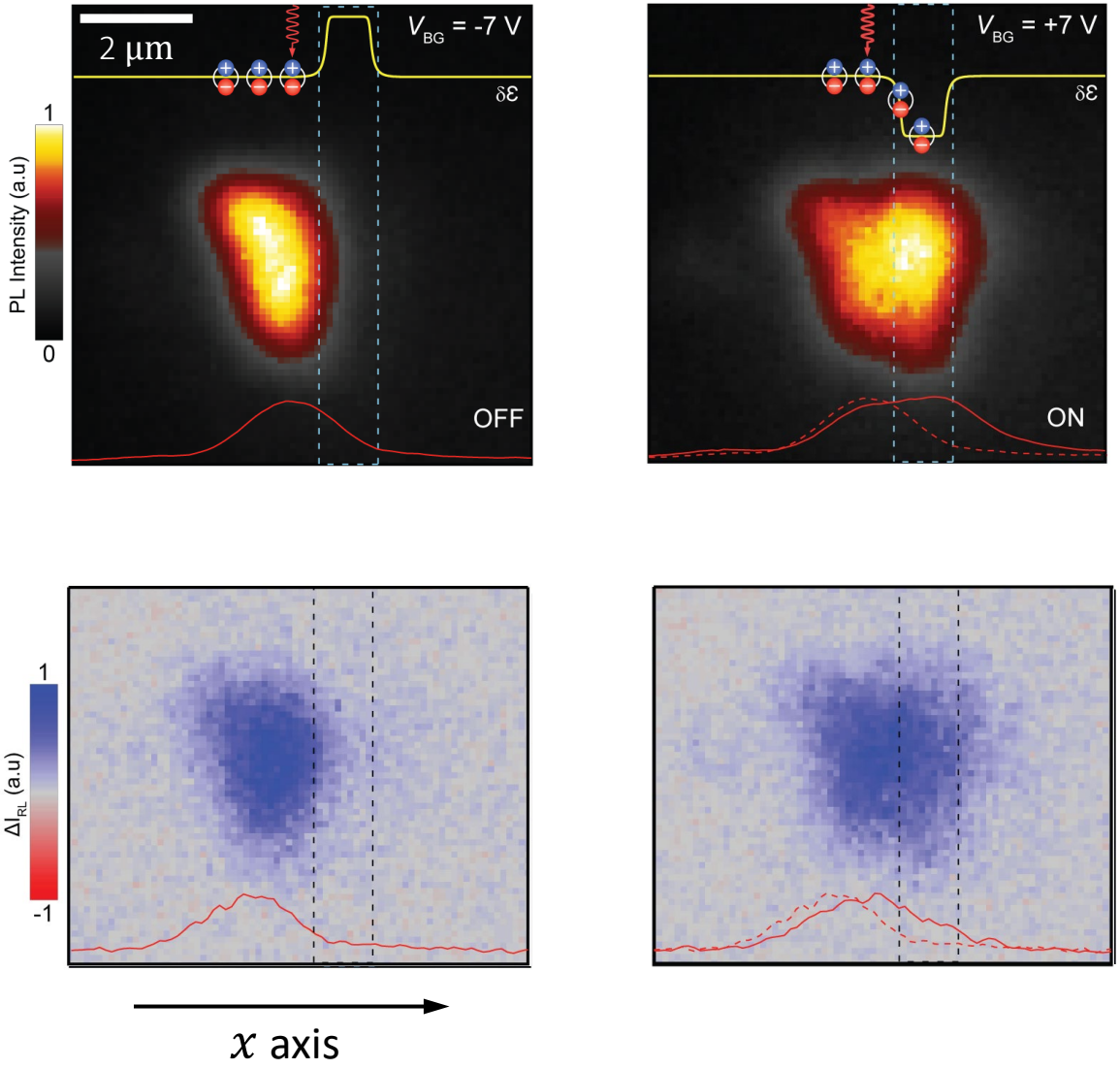


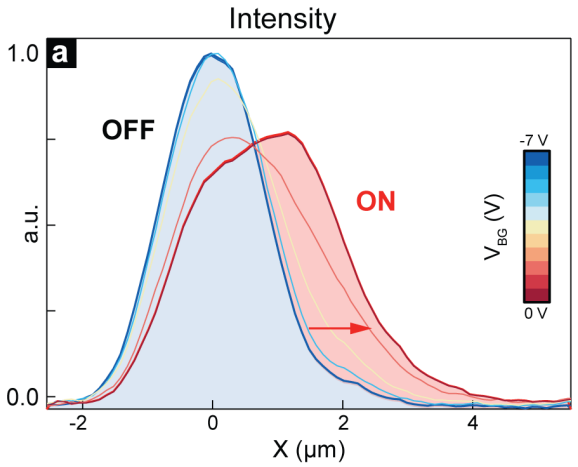
Unuchek, Ciarrocchi…Kis;
Nature Nanotech. (2019)

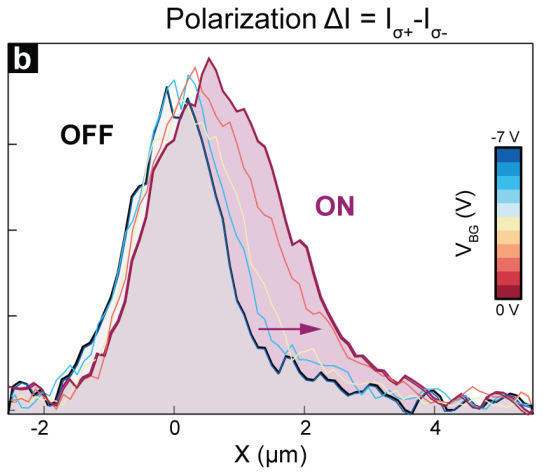
Valley Polarized Exciton Current

OFF state

ON state



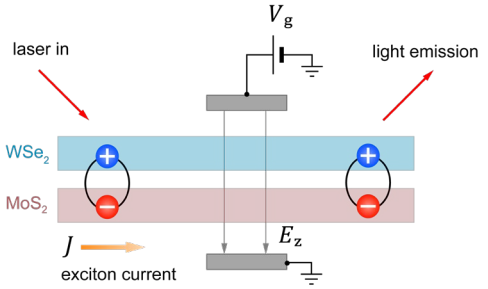




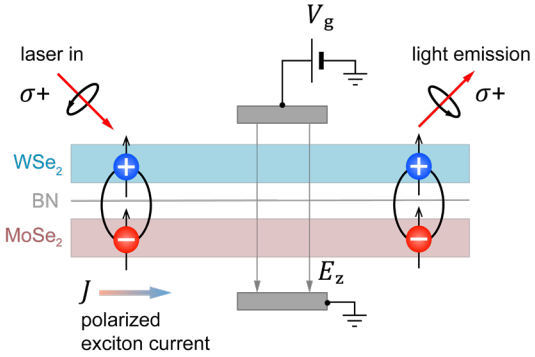
Unuchek, Ciarrocchi…Kis; Nature Nanotech. (2019)

Summary Excitonic Devices

- Room-temperature excitonic devices

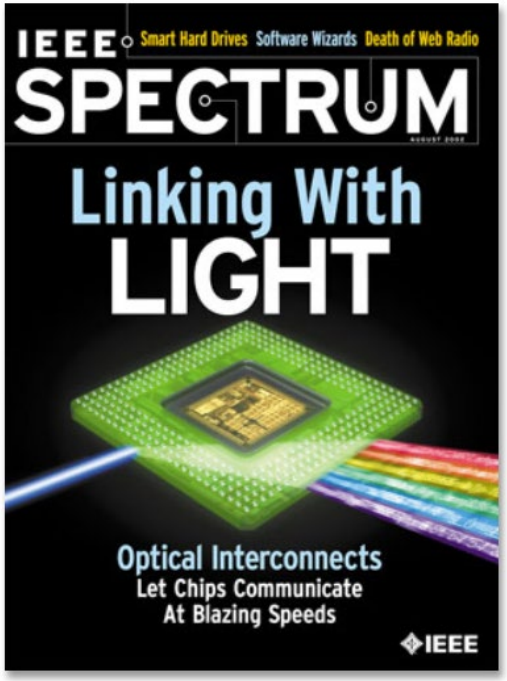


- Valley-polarized excitonic currents

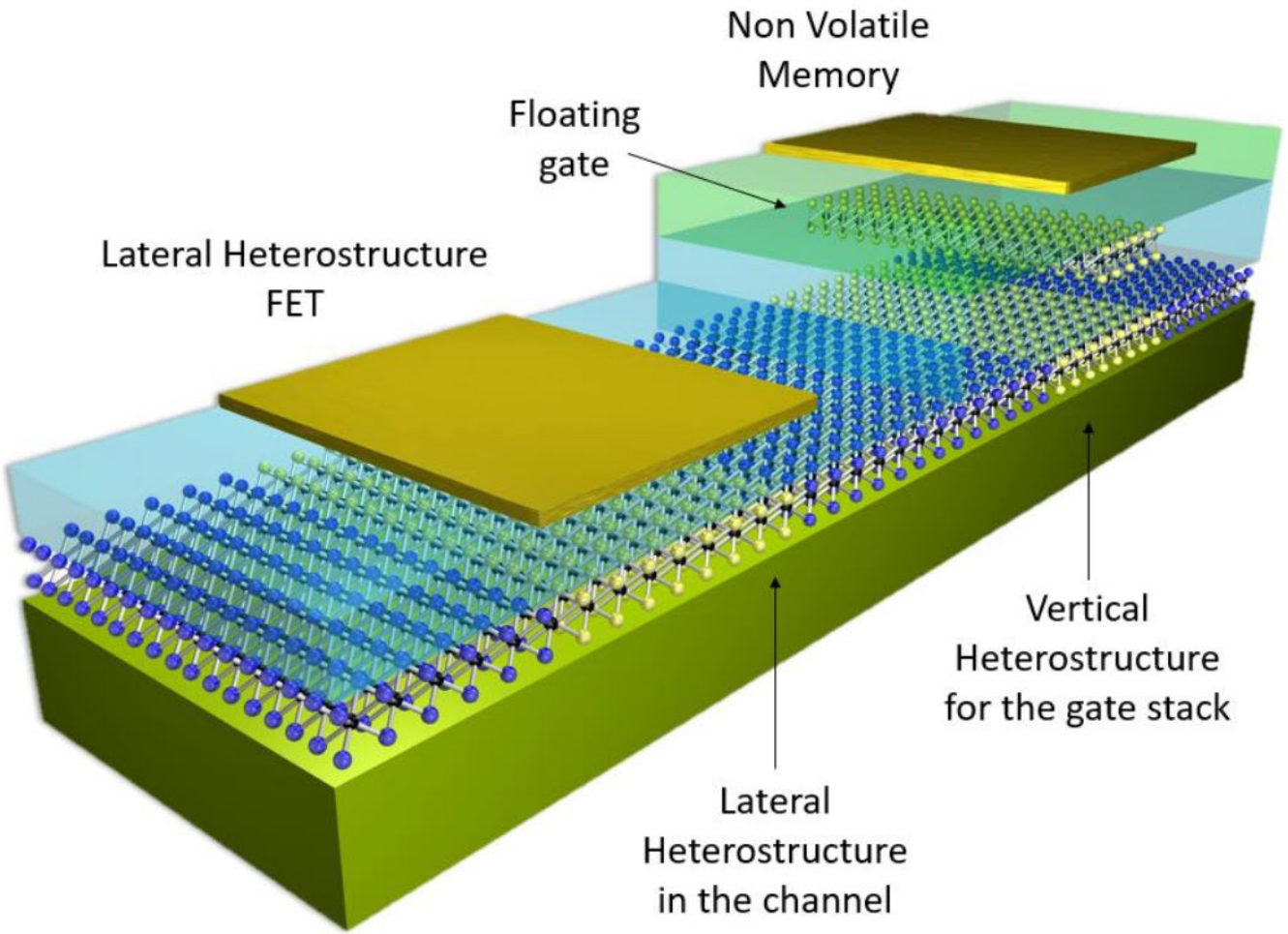


Possible applications

- Excitonic circuits for low-power computing
- Fast and compact optoelectronic components (modulators…)



Logic in Memory Concept

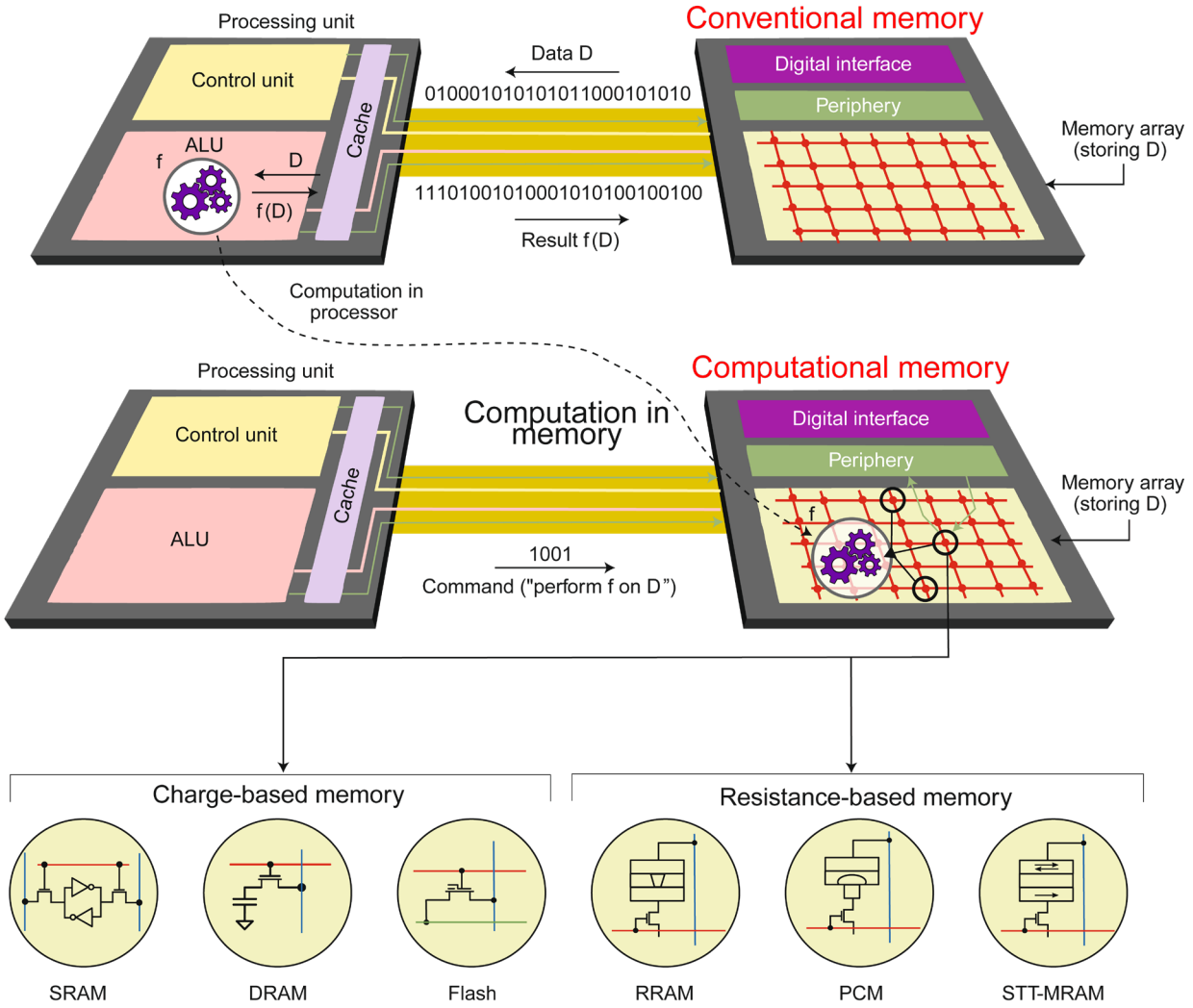


Credit: Giuseppe Iannaccone, University of Pisa

Logic in Memory Concept

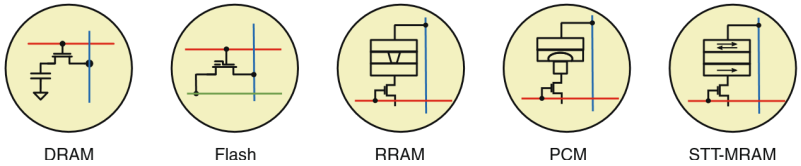
Von Neumann

Logic in memory



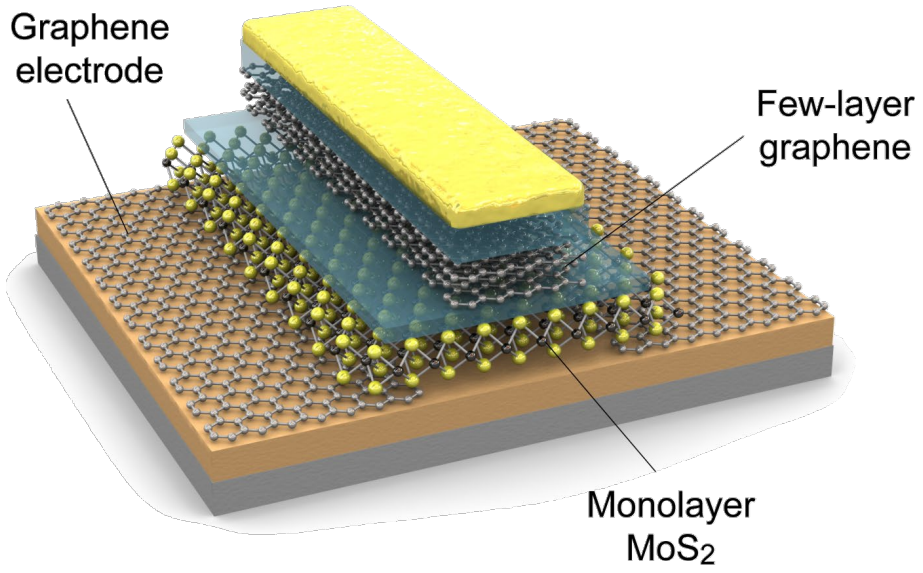
Sebastian…Eleftheriou, Nat. Nanotech. (2020)

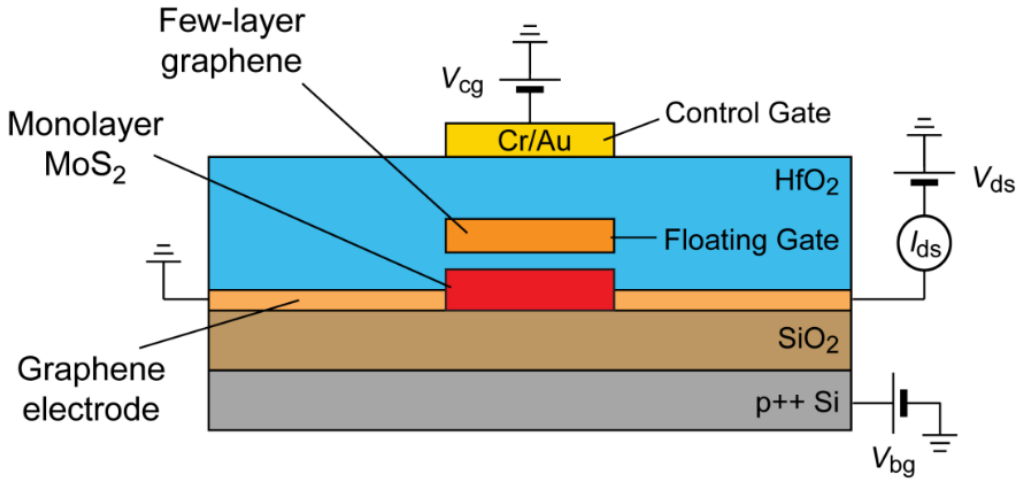
Logic in Memory



Performance metrics	DRAM	Flash	PCM	STT-MRAM	RRAM	HDD
Feature size (nm)	36	22	45	95	9	NA
Cell Area	$6F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	~256*
Write/Erase Time	< 10ns	1/0.1ms	100ns	<10ms	<1ns	5ms
Retention	64ms	>10y	>10y	>10y	>10y	>10y
Endurance	>1E16	1E4	1E9	>1E12	1E12	>1E16
Nonvolatility	N	Y	Y	Y	Y	Y
Multi-level capability	N	Y	Y	N	Y	-
Write Energy (J/bit)	4E-15	> 2E-16	6E-16	2.5E-12	1E-13	-
Standby Power (W/Gb)	1E-1	1E-3	1E-3	1E-3	1E-3	110

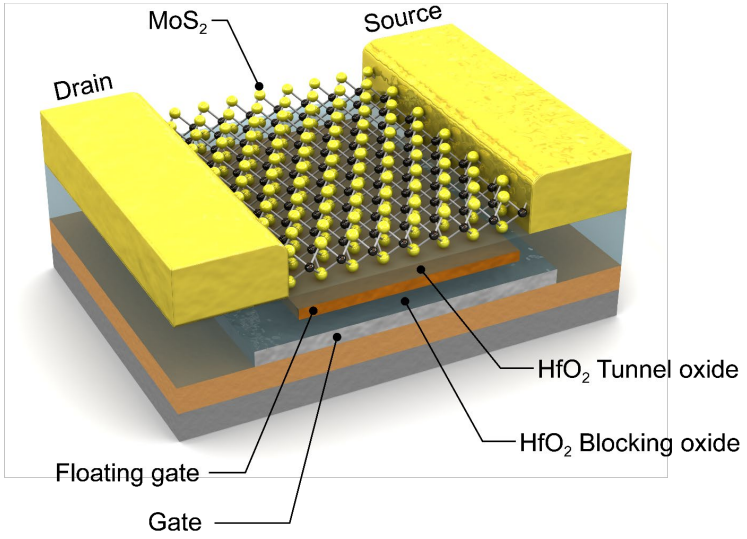
First 2D Flash Memory (2012)

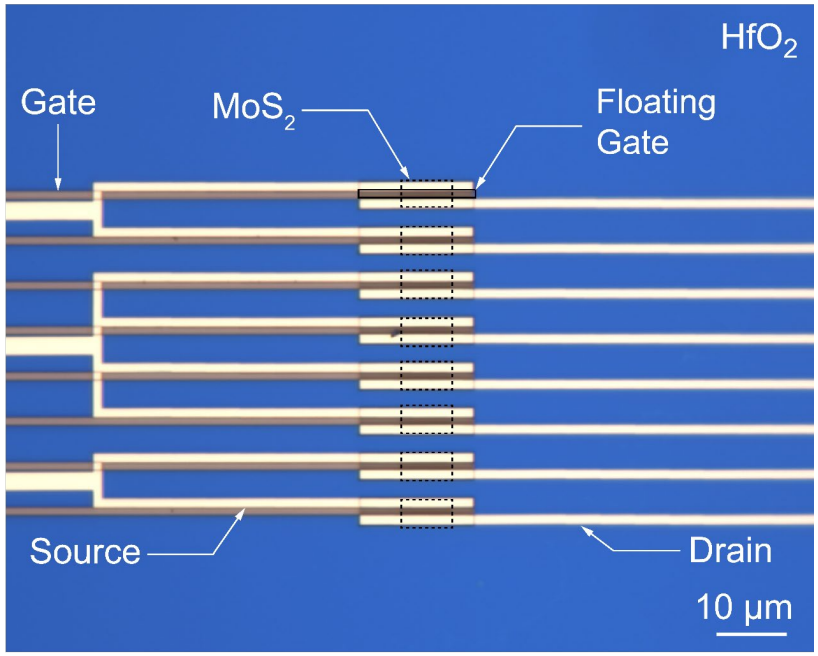


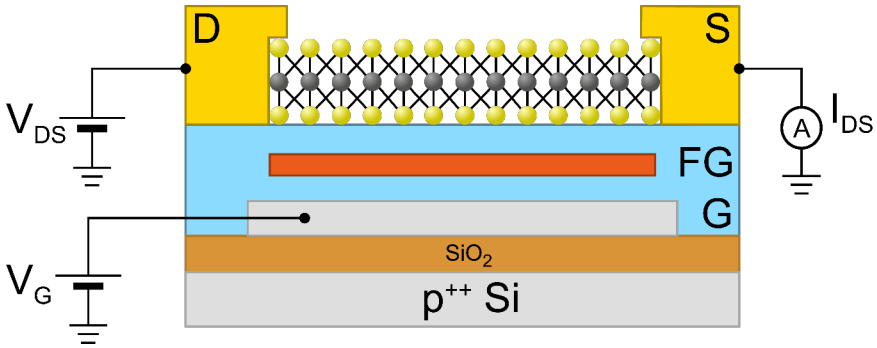


Bertolazzi…Kis; ACS Nano (2013)

2D Logic with Memory



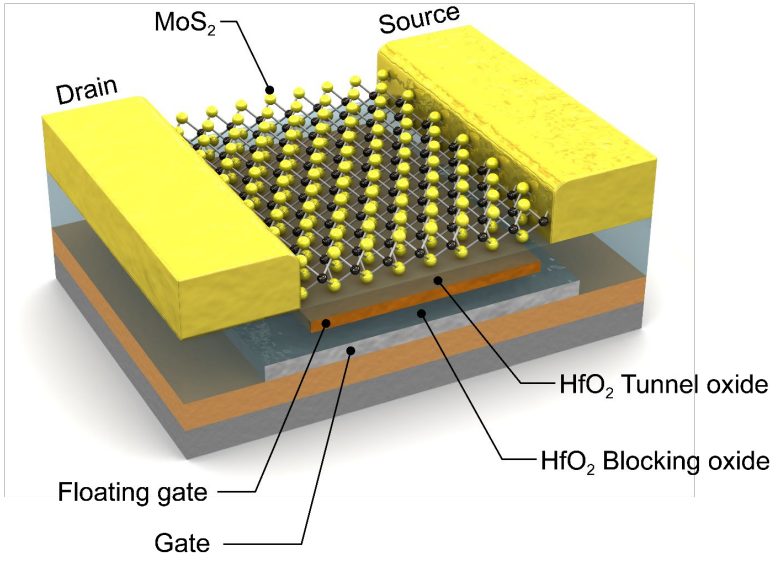


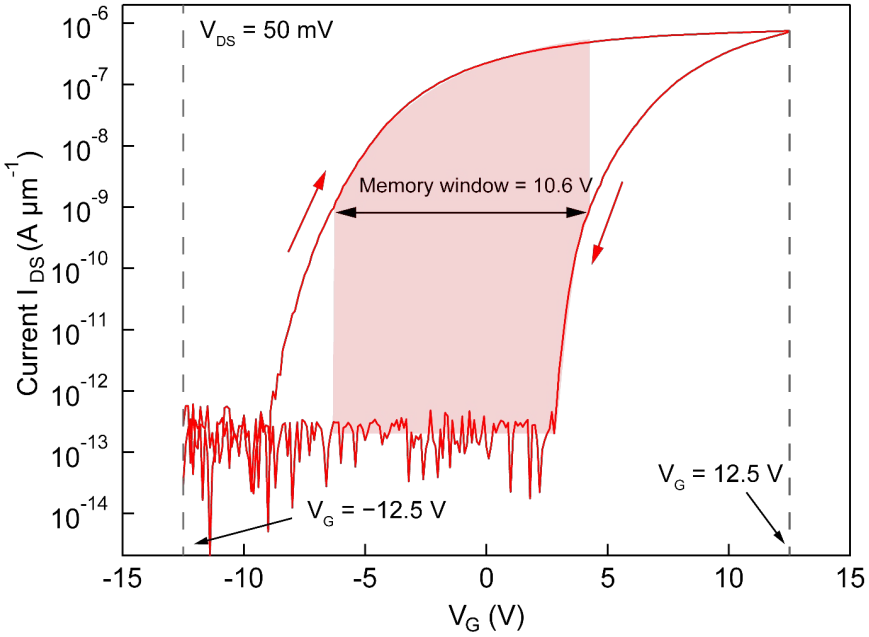


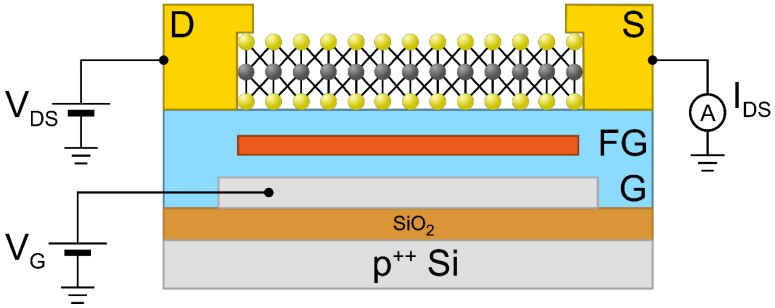
Advantages of 2D for logic in memory and flash memory:

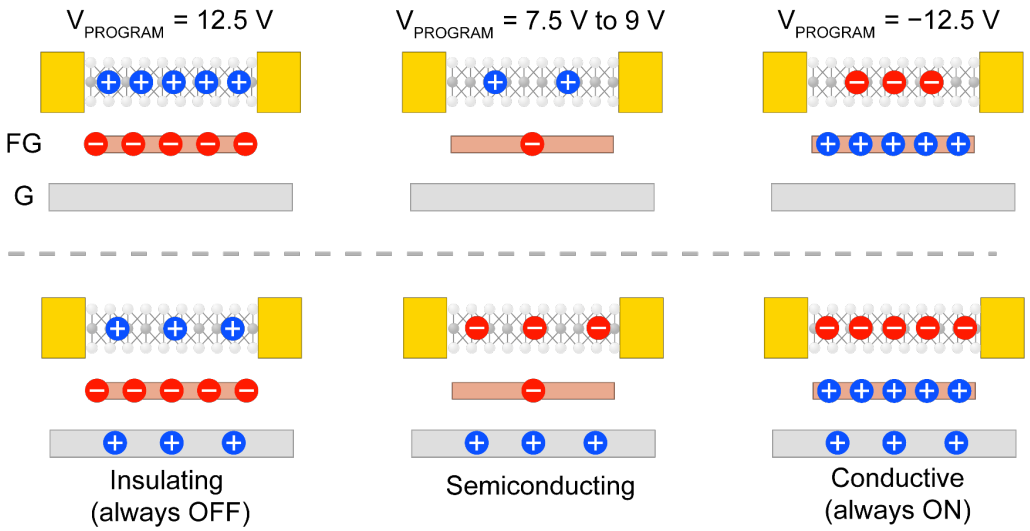
- Reduced cell-to-cell interference
- Multilevel storage
- Possible scaling beyond 12 nm

2D Logic with Memory

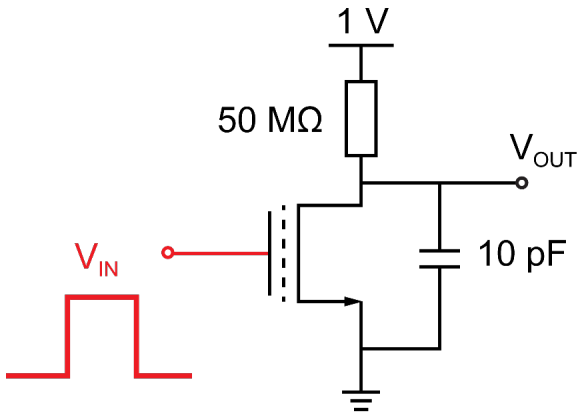








Programmable Inverter

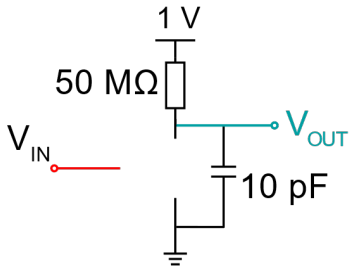


Q	IN		$X^{(Q)}$	
1	0	1	0	0
2	0	1	0	1
3	0	1	1	1

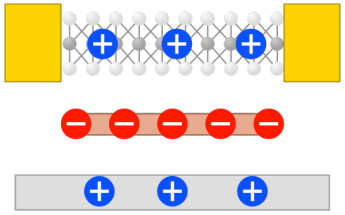
Logic input and memory states

$X^{(Q)}$	OUT
0	1
1	0

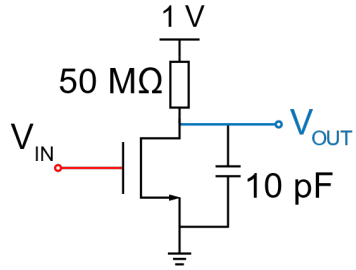
Memory states and logic output



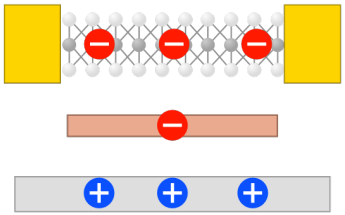
Q = 1 : memory state 0



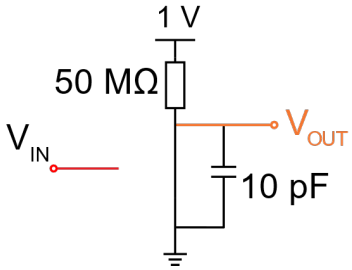
Insulating
(always OFF)



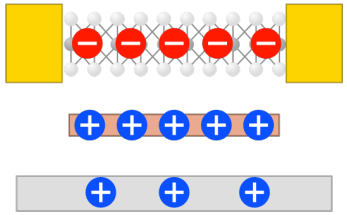
Q = 2 : memory state 0 OR 1



Semiconducting

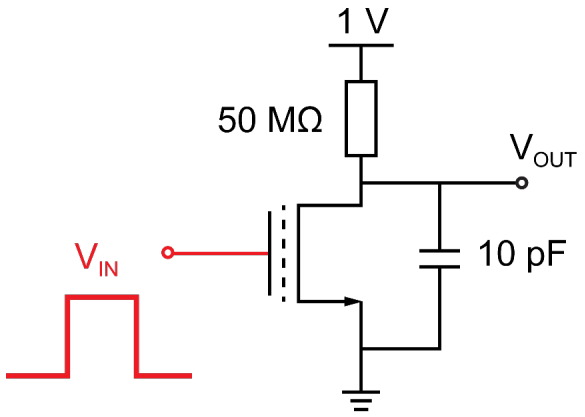


Q = 3 : memory state 1



Conductive
(always ON)

Programmable Inverter

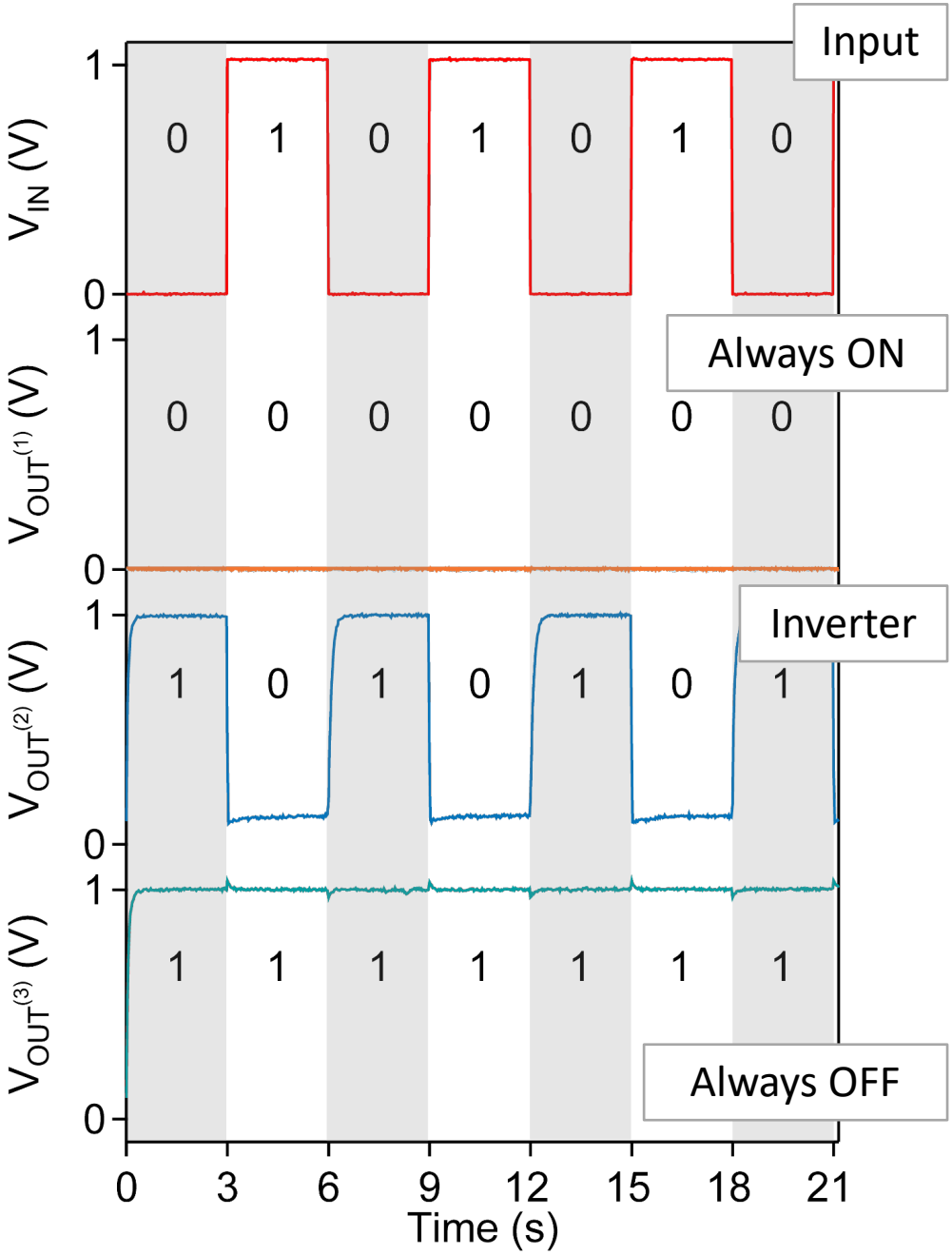


Q	IN		$X^{(Q)}$	
1	0	1	0	0
2	0	1	0	1
3	0	1	1	1

Logic input and memory states

$X^{(Q)}$	OUT
0	1
1	0

Memory states and logic output



Recapitulation

Fundamental limits to power dissipation

- Landauer limit
- Von Neumann architecture
- Joule heating

Emerging concepts based on 2D materials

- Valley/spintronics
- Excitonic devices: currents, polarisation, valley polarisation
- Memory in logic